Approaches to memory integration in large high-performance systems

A. Subramanian S. Iyer
UCLA Center for Heterogeneous Integration and Performance Scaling (CHIPS), Samueli School of Engineering, 420 Westwood Plaza, Los Angeles, CA 90095 (USA)
s.s.iyer@ucla.edu

Modern computing systems are increasingly memory centric in both their architecture, IC content, cost and power. The challenges are (1) density, (2) proximity of memory to processing, (3) retention, (4) reliability, and (5) cost. This has spawned an exciting quest for a universal memory with varying degrees of success. From a practical point of view, we must reconcile ourselves to several of these memories, including the classical workhorses SRAM, DRAM and Flash coexisting with myriad of emerging memories and a rich variety of integration schemes from monolithic integration to heterogeneous integration on a variety of application dependent platforms. In this talk we will trace the evolution of embedded memory and their integration schemes over the last decade or so, and the prognosis for a potential transformation in computing that they may bring about. We will also discuss the use of standard CMOS devices in unconventional operating modes – which we call the Charge Trap Transistor (CTT) – and its potential to make an impact in the memory landscape.