Review

Inorganic Photovoltaics - Planar and Nanostructured Devices


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Abstract

Since its invention in the 1950s, semiconductor solar cell technology has evolved in great leaps and bounds. Solar power is now being considered as a serious leading contender for replacing fossil fuel based power generation. This article reviews the evolution and current state, and potential areas of near future research focus, of leading inorganic materials based solar cells, including bulk crystalline, amorphous thin-films, and nanomaterials based solar cells. Bulk crystalline silicon solar cells continue to dominate the solar power market, and continued efforts at device fabrication improvements, and device topology advancements are discussed. III-V compound semiconductor materials on c-Si for solar power generation are also reviewed. Developments in thin-film based solar cells are reviewed, with a focus on amorphous silicon, copper zinc tin sulfide, cadmium telluride, as well as nanostructured Cadmium telluride. Recent developments in the use of nano-materials for solar power generation, including silicon and gallium arsenide nanowires, are also reviewed.
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1.0 Introduction

The increase in energy demand, decline in conventional energy resources, and carbon
dioxide (CO\textsubscript{2}) emission from fossil fuel sources has prompted research in photovoltaics (PV).

With current total global power needs of 15TW, and with a projection of 30TW by the year
2050 [1], renewable energy is expected to play a critical role in meeting those needs. Among
the renewable energy sources, the PV installation for energy harvesting was about 38.7GW in
2014, and in 2015, the demand rose to about 42.8GW [2]. Nevertheless, despite the
tremendous continuing economic effort on PV research, the total contribution coming from
the PV sector is only about 0.9% [3] of the total global electric energy consumption. In the
first quarter of 2015, the average price for solar cells, modules, and installed utility systems
were $0.31/watt, $0.72/watt, and $1.58/watt respectively [4]. Considering the current global
energy concerns (i.e. insufficient fossil energy supply due to high demand) together with the
problems related to excessive CO\textsubscript{2} gas emission, the huge interest in investing in the PV
sector is obvious. At the same time, if only about 0.1% of the Earth surface were covered
with PV modules with an average efficiency of 10%, this could fulfill the total energy needs
of humanity [5], which provides further impetus to research and development in the PV field.

As a side note, in every second, the sun produces 3x10\textsuperscript{26} W (or J/Sec) [6] of power, in other
words, in every second the sun produces ~500,000 years of our current energy requirements
[7].
Various methods have been developed to harvest energy from the sun that involve capturing and conversion, e.g. solar cells which absorb sun light and convert it into electricity, solar thermal collectors which absorb and convert energy from the sun into usable heat, and wind turbines (wind is an example of solar energy since it is created when the sun heats the Earth) etc. Worldwide electrical energy production is shown in Fig. 1 [3]. Replacing 1kW of electrical energy from fossil fuel sources by PV cells would mitigate CO₂ production [8] by 1 tonne/year. Fossil sources (oil, natural gas, coal) produce CO₂ an average of 260-330g/kWh [9] and 48g/kWh [10] of CO₂ equivalent for PV. The latter is the average of CO₂ equivalent for various technologies such as crystalline silicon (c-Si), multicrystalline silicon (mc-Si), amorphous silicon (a-Si:H), copper indium gallium selenide (CIGS), and cadmium telluride (CdTe).
Among various PV technologies, conventional c-Si p-n junction solar cells currently play a dominant role. These solar cells have improved over the decades and are expected to play a prominent part in solar power generation for the foreseeable future. However, the cost-per-watt peak ($/W_p$, the term “peak” refers to peak sun hours – global average of about 5 hrs/day) of c-Si solar cells are still relatively high. High-efficiency and reduced production costs are crucial factors to achieve grid parity (cost of PV generated electricity on par with grid electricity known as grid parity). There are two approaches for low-cost (i.e. low $/$Wp) c-Si solar cells: (i) lower the cost using cheaper consumables such as spin-on sources for doping [11,12], low cost metallization schemes, thinner wafers and lower quality Si feedstock etc., and (ii) increase the cell efficiency by using selective emitters, local back surface fields etc., in front junction cells, or by using an interdigitated back contact structure in back junction cells. In the back contact structure, the p-n junction lies at the rear side of the c-Si wafer, and no contact grids are present at the front side. Therefore, the losses due to shadowing are eliminated, which results in an increase in short circuit current and efficiency. For c-Si based front junction and back junction solar cells, the metal/c-Si interface regions are sites of high electron hole (e-h) recombination rates, and this affects efficiency. In the case of front (a-Si/c-Si) heterojunction, and back (a-Si/c-Si) heterojunction (BHJ) cells, the metal/a-Si interface is electronically separated from the c-Si bulk by inserting an intrinsic a-Si:H layer, which also acts as a passivation layer to c-Si. A BHJ solar cell is a combination of front heterojunction and back junction cells. In the BHJ design [13,14], shadowing loss can be avoided completely due to a grid-less front side; an interdigitated pattern of p- and n-type contacts collects the photogenerated current on the rear. In thin-film solar cells, fabrication of a-Si:H cell is relatively simple with low fabrication cost [15]. However it also comes with lower performance. Efficiency of thin-film heterojunction solar cells such as CIGS, copper-zinc-tin-sulfide (CZTS) and CdTe based cells lie in between c-Si based cells and a-Si:H cells.
Nanowire (NW) solar cells such as Si nanowire (SiNW) [16] and gallium arsenide (GaAs) have recently caught research attention. While optical absorption may be low in individual NWs, the use of mats or forests of NWs in a solar cell potentially may overcome that issue. Optical absorption is also potentially increased through light-trapping in those forests. NWs may be used in different ways in a solar cell, which provides greater options for design. They also lend themselves to flexible solar cells, an important current research focus.

In this article, we review inorganic wafer based solar cells that include c-Si based solar cells- front junction, back junction, front heterojunction, and back heterojunction. We also review multi-junction (III-V or perovskite on c-Si) solar cells, and thin-film solar cells, viz. a-Si:H, CZTS, and CdTe based solar cells. Apart from planar devices, cadmium sulphide (CdS)/CdTe, SiNW, and GaAs nanostructured solar cells are reviewed. We present current developments in R&D, existing problems that need further research, and identify some points where research is stagnant. We provide explanations to the problems associated with different solar cells. Limiting factors for efficiency and how to improve efficiency are discussed. Current challenges and possible strategies to overcome those challenges are mentioned.

2.0 c-Si based solar cells: Front junction

In this section, fabrication of conventional aluminum (Al) back surface field (Al-BSF) solar cell is reviewed in detail. Other types of solar cells, such as passivated emitter rear contact (PERC), passivated emitter rear locally-diffused (PERL), metal wrap-through (MWT), and emitter wrap-through (EWT) cells are also discussed. Low-cost approaches for producing cheap wafers, doping and metallization are outlined.

2.1 Historical approach: Evolution of the c-Si solar cells to present

The photovoltaic effect was first observed in 1839, when Becquerel [17] produced a current intensity by exposing silver (Ag) electrodes to radiation in an electrolyte. Later, in 1877, Adams and Day observed that the exposure of selenium (Se) electrodes to radiation
produced electric voltage and current [18]. However, no significant research was reported on
the photovoltaic effect until 1949 when Shockley [19], Bardeen, and Brattain [20] reported
their work on the transistors and the physics of the p-n junction. The history of the modern
PV started at the Bell Labs in USA in 1954 when researchers, realized that p-n junction
diodes produced voltage under illumination. One year after this discovery, Bell Labs
produced a c-Si p-n junction solar cell with 6% efficiency [21]. In 1960, several authors
developed the fundamentals of the p-n junction solar cell and the relations between bandgap
(hereafter $E_g$ or bandgap), incident sunlight dependence, the influence of temperature,
thermodynamics of the solar cells, efficiency limits, etc. In 1961, Shockley and Queisser [22]
reported the maximum theoretical efficiency of 29% (known as Shockley and Queisser limit
or S-Q limit) using a p-n junction solar cell, establishing the basis to understand the
performance of the solar cells and the losses mechanisms.

The first world oil embargo was instituted on 1973 by the Persian Gulf oil producers.
This incident produced a strong impulse for PV as many governments from industrialized
countries began programs to develop renewable energy and to reduce the oil dependence.
Consequently, the terrestrial application of photovoltaics was reinforced. During the 1980’s,
the industry started producing Si PV modules, focusing in scaling up the fabrication systems,
the manufacturing processes, and reinforcing the cost analysis [23].

In 1985 the first high-efficiency c-Si solar cell under standard measurement
conditions was reported by University of New South Wales, Australia [24]. In the 1990’s, the
use of solar cells for commercial purposes was extended. In 1995, a German project
demonstrated the use of PV installation on roofs, favoring PV legislation in Germany, Japan
and several countries encouraging the introduction of PV systems at homes. In 1997,
worldwide PV production reached 100MW, and in 1999 the cumulative worldwide installed
photovoltaic reached 1000MW. The annual production in 2014 has increased to 45GW
(reported production vary between 39 and 49GWp), and the accumulated power installed around the world has reached 183GWp at the end of 2014 [25].

As shown in Fig. 2, the solar cell market is led by standard crystalline technology, using single-junction solar cells, with 92% of the total market. Other technologies such as CdTe, CI(G)S, and a-Si:H thin-films etc., make up the rest [26].

Single-junction c-Si solar cells present several advantages [27]. Si is an abundant non-toxic material, composing about a 25% of the Earth’s crust, and c-Si based photovoltaic modules are long-term stable outdoors, with a lifetime longer than 20 years. The current technology has relatively high energy conversion efficiency in comparison with many other technologies and lower system costs. This enables installation of high-power systems. As we will also discuss, single-junction technology still has a considerable potential for further cost reductions.

On the other hand, the disadvantages of this technology include a limitation to substantially increase the efficiency of the solar cells, as it is already close to its technical limit. Moreover, at the present, fabrication of solar cells requires high-temperature and energy. A large amount of Si is required for the wafer, and the wafering process (accounts for 22% of the entire production cost of c-Si cell) [28] itself wastes approximately the 50% of the Si ingot. The wafers are also very fragile. At a broader level, the c-Si solar cell technology currently requires the support of three different factory equipments for wafer, cell, and module production, and several times its integration in a single factory is not easy, which in turn can affect the overall business if competitive prices are required.
Fig. 2 Market share of different solar cell materials in 2014 showing the dominance of c-Si (92%) followed by CdTe [26]. In the case of a-Si:H solar cells, the main issue with a-Si:H, light induced degradation, has not been solved so far. For CdTe solar cells, cadmium is abundant and tellurium is not abundant. CdTe is less toxic than cadmium and disposal of CdTe solar panel is an issue in the large-scale commercialization since CdTe modules pollute during decommissioning. CdTe disposal is a major concern in developing countries. As a side note, in the middle and late 1980s, the use of indium tin oxide in LCD products has increased indium demand and price rose to several hundred dollars per kilogram. Similarly, the demand for indium may increase with large production of CIGS based solar cells, and may results in unstable price in CIGS module.

Considering the Carnot limit for a solar cell and due to the temperature of the Sun, the thermodynamic efficiency limit is about 86%. However, this limit is only calculated in terms of the working temperature of the system. As mentioned above, in 1961 the first study on the efficiency limit of a solar cell was calculated [22] using a detailed balance. In that work the electron generation due to the absorbed photons and radiative recombination was analyzed. This efficiency limit was calculated for solar cells based on a semiconductor with a valence and a conduction band separated by bandgap. This study has several assumptions: (i) there is only one semiconductor material per solar cell, (ii) there is only one p-n junction per solar cell, and (iii) the sunlight is not concentrated and all the energy is converted to heat from photons with energy larger than the bandgap. The result of this calculation indicates that there is a maximum efficiency of 33% for any type of single-junction solar cell. The limitation in
the efficiency is due to the 47% of the solar energy directly converted to heat, 18% not absorbed by the solar cells and 2% lost in local recombination. However, according to S-Q limit, a maximum efficiency of 29% can be obtained [22, 29, 30].

The evolution of the single-junction solar cells technology has been extensively discussed [31]. Since the early 1950s there have been important milestones in the field. In Bell Lab the first cells were fabricated on p-type c-Si and they showed efficiencies of around 4.5%. Using arsenic-doped n-type c-Si with a boron-doped emitter [21], the efficiency reached values above 6%. In the early 1960s, due to requirements of solar cells for space flights, p-type c-Si with a phosphorus-doped emitter was developed [32]. The second important improvement occurred at the beginning of the 1980s, when the PERC solar cell was produced. This reached 20% efficiency in 1985 [33]. Currently, the efficiency record for p-n junction c-Si is ~25%, which was reached in 1998. For mc-Si the efficiency is 21.25% (area 156x156 mm²) which was reached in 2015 [34]. There has been no change in the maximum efficiency for c-Si and mc-Si solar cells, from 1998 and 2004 respectively. However, in the industrial production line, some steps as new texturization methods (to increase photons absorption), local BSF, and selective emitter have been included by the most important production lines manufacturers to increase the average commercial efficiency to 19% for c-Si and 18% for mc-Si. One of the challenges of the industry and also one of the reasons to review this section is to describe how these advances have been transferred from laboratory to production scale, allowing at the same time high-throughput and high-efficiency in the solar cells. Current challenges for this technology are the implementation of new concepts to target and reduce the loss mechanisms.

Recombination losses can be reduced using new passivation layers and chemical processes. However, from the point of view of the industry, most of these techniques are not cost-effective due to the requirement of high vacuum and energy. Also the process times are
not affordable to accomplish a competitive industry production. On the other hand, light not absorbed can be reduced using multiple anti-reflection coatings (ARCs), or including other absorber materials. Both strategies have not been integrated in the industrial production lines due to their high cost. In our opinion, these strategies should be subject of increased study in the future.

### 2.2 Conventional c-Si based solar cells

To understand the single-junction solar cell fabrication steps, it is necessary to first understand the device structure. A schematic diagram of a simple p-n junction p⁺-p-n⁺ type solar cell is shown in Fig. 3. At the rear side, a heavily Al-doped p⁺-region (Al-Si alloy) in p-type c-Si forms a high-low (p⁺/p) junction known as Al-BSF. The thickness of the Al-BSF region is around 0.2 μm. The phosphorous diffused emitter thickness is around 0.8 μm. Detailed fabrication steps are mentioned in Sec. 2.3.

![Schematic diagram of p⁺-p-n⁺ type solar cell having Al-BSF](image)

Fig. 3 Schematic diagram of p⁺-p-n⁺ type solar cell having Al-BSF [27]. Solar cell works as follows: Incident light generates electron-hole pairs in the p-type c-Si absorber. Due to built-in electric field across the p-n junction, electrons travel towards the n-type electrode and are in turn collected by the grid electrodes. Holes, on the other hand, travel across bulk c-Si and are collected by the Al back electrode. The potential barrier at the high-low (p⁺/p) junction provides an additional mechanism to drive electrons away from reaching the back electrode and towards the p-n junction. This increases $V_{oc}$ and $J_{sc}$ due to reduced back surface recombination [11].
The wafer size used commercially has been increasing over the years. For a considerable length of time, the Czochralski Si (Cz-Si) wafer diameter was 4” as it was the standard size in the microelectronic industry and the Si wafers came mainly from stocks offering quality standards just under those accepted by the microelectronic industry. Then, due to the microelectronic industry requirement, and subsequently to the photovoltaic industry requirement, the wafers have passed from 10x10cm$^2$ (4”x4”) to the current standard 15.6x15.6cm$^2$ (6”x6”). The wafer also has evolved from circular to pseudo-square and to square shape to maximize the solar module active area. A pseudo-square wafer comes from a circular wafer where the inner square is obtained showing the typical 45º cut corners.

In the case of mc-Si, the manufacturers have been offering square surfaces since the beginning because of the fabrication procedure. The thickness of the wafer has been reduced over the last decades to save Si, as it is the main component of the Si solar cell cost. Thus, from 500µm at the beginning of the 1990s, currently the wafer thickness is around 180-220 µm [35]. There has been considerable research activity in relation to further reductions of wafer thickness to save Si, and to obtain flexible properties for the wafer. However a reduction in the wafer thickness may also result in reduction of the efficiency and yield of the final solar cell unless appropriate light trapping and surface passivation solutions are implemented.

The base doping level of the wafer is around $10^{16}$ atoms/cm$^3$, which correspond with a resistivity of $1 \, \Omega \cdot \text{cm}$. This doping level is related to the optimum recombination properties of the wafer to improve the cell efficiency.

Currently, the c-Si PV market is dominated by p-type Si wafers. However p-type wafers are sensitive to chemical impurities that can be activated in high-temperature processes, resulting in efficiency loss. P-type c-Si solar cells possess degradation of minority-carrier lifetimes induced by illumination or carrier injection [27]. This lifetime degradation is
stabilized after one day, which concomitantly also produces a degradation of the solar cell efficiency. In some cases, depending of the wafer quality, this degradation can reach 1% of the total efficiency. This effect is clearly related to the presence of boron and oxygen. N-type c-Si solar cells are an alternative to avoid the carrier-induced degradation of p-type c-Si, as the former do not present this effect, even when high concentrations of oxygen are detected in the Si wafer. This difference is related with the ratio of electron to hole capture cross sections of the corresponding defects, which is greater than unity. Therefore, n-type c-Si wafers have higher minority-carrier lifetime and hence higher minority-carrier diffusion length for the same concentration of impurities present in bulk Si.

A passivation layer on the crystal surface is used to reduce surface defects. In addition the front side of the wafer is normally textured in order to improve the absorption of the incident radiation. Also the front surface is doped with phosphorus to form the p-n junction. The phosphorous surface concentration is around $2 \times 10^{20}$ atoms/cm$^3$, with a sheet resistivity ($R_{sh}$) between 50 and 75$\Omega$/sq. The front side is a $\lambda/4$ (where $\lambda$ is wavelength of light) coated thin layer of amorphous hydrogenated SiN for an effective reduction of front reflection. Finally the metallic contacts are placed by the screen printing technique: Ag is placed in the front side, with a finger and busbar structure to allow solar incident radiation to the emitter, and fully covered by an Al back side contact. The paste used must be dried and fired to produce a proper Ohmic contact [36]. The solar cells are edge isolated (Fig. 4) in order to avoid contact between front and the back side during the fabrication process.

In the standard cell process, the metal impurities can be reduced and even totally deactivated when the wafers are submitted to the diffusion process, due to gettering effects (explained in Sec. 2.3.3.). Below we review briefly on raw materials and wafer production technology.
Fig. 4 Solar cells are edge isolated on both sides to avoid shunting between top and bottom contacts [37]. Edge isolation is performed by plasma etching, laser or laser scribing or chemical etching. In plasma etching, solar cells are coin stacked and then edges are etched away using plasma. If edge isolation is not performed, phosphorous diffusion on the edges provide short circuit to electrons and reach back electrode. For efficient solar cell operation, very high shunt resistance is required.

2.2.1 Raw materials

There are several processes involved in reaching the desired purity of c-Si for solar applications. To obtain solar grade Si, it is necessary to produce metallurgical grade Si (mg-Si) with a minimum of 98.5% Si content [23]. Mg-Si is produced by the introduction of the raw material in electric arc furnaces with quartz and carbon materials. The following reaction occurs:

\[
\text{SiO}_2 (s) + 2C (s) \rightarrow \text{Si} (l) + 2\text{CO} (g)
\]

where SiO2, C, CO are silicon dioxide, carbon and carbon monoxide respectively.

To carry out above reaction, lumpy quartz with appropriate purity and thermal resistance is required. The refined liquid Si is decanted from the ladle into a cast iron mold or onto a bed of Si fines. The casting should be removed from the mold while it is still not fully solidified. In this step, the mg-Si becomes mc-Si. This is smashed to obtain pieces of around 10cm. There are several processes [23] to produce electronic grade Si of highest purity.
The most frequently used process is based on the decomposition of trichlorosilane (TCS) with temperatures around 1100°C on a heated Si filament placed in a deposition chamber. This process is called Siemens process [38].

### 2.2.2 Wafer technology description: Cz, Fz, and mc-Si

When the literature refers to crystalline Si, one (or more) of three different materials is implied: the Cz-grown c-Si, float-zone (Fz c-Si), and mc-Si. C-Si ingots are formed by Cz process, based on the melting of electronic grade Si and using a rotating Si seed. The ingot is formed when the seed is pulled out of the crucible [23]. The cooling down process is critical to obtaining high quality Si ingot. The rotation velocity can be adjusted to obtain different sizes.

The floating zone process is performed on polysilicon rod to convert polysilicon into single crystal Si ingot. In this process, seed crystal plays an important role. By heating one end of the rod, seed crystal is fused and then seeded molten zone is passed through the length polysilicon rod to convert it into single crystal Si ingot.

Directional solidification is the conventional method for producing mc-Si ingots. Si seed crystal is not used to produce mc-Si ingots. In this method, Si scrap is used as the starting material. After melting the starting material, molten Si is poured into a square shaped crucible. By cooling, directional solidification takes place and large crystals grow in a random direction. The mc-Si technology presents several advantages with respect to the Cz-Si technology: (i) the fabrication procedure is easier, (ii) lower manufacturing costs, and (iii) higher feedstock tolerance. Also, the mc-Si wafers are rectangular or square yielding a larger utilization of the module area in comparison with round or pseudosquare Cz-Si or Fz-Si wafers. However, as compared to Cz-Si and Fz-Si, mc-Si has much higher defect content, which reduces the expected efficiency of the solar cells. Consequently, as the spot price of c-
Si and mc-Si varies in the market and different wafer qualities can be purchased, it is not easy
to define the best wafer option for producing Si-based solar cells.

2.3. Fabrication of Al-BSF c-Si solar cell

The Al-BSF solar cells concept includes several physical structures with slight differences. In
the following flow chart (Fig. 5), the main steps are depicted.

Fig. 5 Processing steps for front junction c-Si solar cell. Since electron mobility is about three times higher than
the hole mobility, conventional solar cells are fabricated on p-type c-Si wafers for easy minority (electrons)
carrier collection. Also, it is easy to obtain high-quality phosphorous diffusion than boron diffusion. However,
boron-oxygen complex formation in Cz p-type c-Si reduces minority-carrier lifetime. In production, Fz c-Si
wafers are used due to less oxygen content in Si wafer. An ideal resistivity and thickness of c-Si are 0.5\(\Omega\)-cm
and 180-200\(\mu\)m. For larger resistivity values, Al/p-Si interface becomes rectifying contact (Schottky barrier)
and reduces \(V_{oc}\) and fill factor due to narrow depletion width of schottky junction [39]. Energy payback time
[40] for c-Si solar cell is \(\sim\)2 years.

Passivation of the front side is very important to obtain high-efficiency. To reduce
surface recombination velocity (SRV) at the rear side, it is necessary to carry out passivation
using a \(p^+\)-layer, otherwise the solar efficiency will decrease dramatically. The easiest
procedure to obtain the $p^+$-layer in the rear side is using boron doped Al paste to avoid high recombination velocities in the rear side of the solar cell. This process is called Al-BSF [27].

### 2.3.1 Cleaning process

Cleaning process and the environmental control is critical to avoid contamination and to allow high-efficiency. Several cleaning processes have been commonly used in R&D, depending on the purpose. Radio Corporation of America (RCA) cleaning procedure [41] is the standard process for removing contaminants from Si wafers. It consists of two steps:

(i) RCA 1 is used for organic cleaning. Organic contaminants are dissolved by immersing c-Si wafer in a solution containing de-ionized (DI) water having resistivity of about 19 M$\Omega$·cm, ammonium hydroxide (NH$_4$OH) and hydrogen peroxide (H$_2$O$_2$) in the ratio of 5:1:1. NH$_4$OH is added to DI water and finally H$_2$O$_2$ is added. To remove organic residues, the wafer is treated in the bath at 80°C for 15 min. This process oxidizes Si and leaves a thin oxide on the Si surface that can be removed if pure Si surface is required.

(ii) RCA 2 is used to remove metal ions from c-Si wafer. The solution contains DI water, hydrochloric acid (HCl) and H$_2$O$_2$ in the ratio of 5:1:1. HCl is added to DI water and then finally H$_2$O$_2$ is added. This clean is performed around 90°C for 15 min.

Note that, to our best of knowledge, RCA cleaning process is not used in industry to reduce production cost and to avoid the need of recycling chemicals. Before saw damage removal, soap solutions are used to clean wafers.

### 2.3.2 Saw damage etching/texturing processes

The sawing process generates a high degree of damage on the “as-cut” surfaces, producing a low quality surface with a large amount of defects on it [42]. These defects can produce fracture during the solar cells processing and lower the performance of the solar cells [43]. Thus, one of the necessary steps to obtain high-efficiency Si solar cell is to introduce
saw damage etching of the wafer at the beginning of the fabrication process, and it is carried out by immersion of the wafer in a chemical solution [27].

Optical losses of the solar cells can be improved by means of a texturing process on the front surface of the Si wafer [36]. The aim of the texturing process is to produce a specific morphology on the Si surface able to redirect reflected light into the device to improve the light absorption, i.e., diminish the reflection losses from the front surface. To carry out texturing, several methods are available, such as mechanical grooving [43,44], reactive ion etching (RIE), anisotropic alkaline etching [43], acidic etching [45], chemical etching using a metallic catalyst [46], dry etching processes as plasma texturing [47], and laser texturization [48]. Among these methods, wet chemical etching is the mostly used in industrial process and commercially it is also the most commonly used procedure for c-Si solar cells. This is because of its low-cost, high etching rate, and large-area uniformity [49]. Saw damage etching and the texturization process can be carried out in the same step when chemical solutions are used.

For c-Si, pyramid formation is due to anisotropic etching resulting from the difference in etching rates for the <100>, <111> planes of c-Si. The pyramids size and height are highly depending on the etchant and the etching parameters [43]. Mixed alkaline solutions, such as a sodium hydroxide (NaOH) or a potassium hydroxide (KOH) solution, with isopropyl alcohol (IPA) are used to texture the monocrystalline Si surface. However, IPA cost limits the use of these solutions. For chemical anisotropic etching, the solutions without IPA have been acquiring more relevance during recent years [50, 51]. Cheaper alternative solvents are sodium carbonate (Na$_2$CO$_3$) [52], potassium carbonate (K$_2$CO$_3$) [53] and sodium phosphate (Na$_3$PO$_4$) [54].

Recently a mixture of Na$_2$CO$_3$ and sodium bicarbonate (NaHCO$_3$) has been optimized. This has significantly reduced the amount of the solvents and their costs [43], and
has proved to be the most promising to be used in c-Si texturing processes. Another chemical used to perform wet chemical etching is tetramethyl ammonium hydroxide (TMAOH). It is also a cost-effective procedure and does not produce metal contaminations on the wafers [51].

As mc-Si is composed of several Si crystals or grains with different orientations, anisotropic etching cannot be applied efficiently for random pyramid texturization. For this reason, isotropic etching in acidic solutions is the most cost-effective procedure to texture mc-Si wafers. Acidic texturing is normally based on solutions containing hydrofluoric acid (HF) and nitric acid (HNO₃) in acetic acid (CH₃COOH) or DI water [55, 56]. Also vapor etching using these solutions [57] has been applied because of a resultant enhanced etching rate control. Other alternatives to control the etching rate, such as NaOH/sodium hypochlorite (NaOCl) based solutions, have been reported [58]. For mc-Si wafers, the challenge is to find out a reproducible process to decrease the reflectance and to increase the photocurrent. The research is currently focused on RIE processes [59].

In addition to traditional approaches to texturization, several alternatives have also been developed. Laser texturing, lithography and plasma texturing are mainly used in laboratory scale due to their cost and requirements [45]. Laser texturing is a promising technique to obtain nanostructured surfaces under certain illumination and power conditions. The types of surfaces obtained are known as black Si [60]. Using a femtosecond laser a reduction of the reflectance to around 3% when this is used [61] has been reported. Recently a two-step laser surface texturing process has been proposed and studied, where a high-fluence laser ablation step was followed by a low-fluence laser-induced melting, producing a molten material flow and re-solidification step to smooth the ablated dimple bottom surface [62]. This study shows that the two-step laser surface texturing process can produce micro dimples with very smooth bottom surfaces.
Plasma texturing, also called RIE, includes lithographic techniques in some cases. This technique encloses different approaches as selective etching through alumina template, SiO₂ micro-masks, catalytic action of various metals and nano-imprint lithography. These approaches have been developed for the fabrication of sub-wavelength structure surfaces that act as black Si.

2.3.3 P-N junction formation: Doping from solid/liquid/gas sources

When p-type wafers are used as base material, phosphorus incorporation on front side of c-Si is performed to obtain p-n junction. There are several methods to carry out the step, diffusion and ion implantation being the most usual processes. The obtained doping profiles are highly dependent on the used technique. Doping by ion implantation is mentioned in Sec. 2.5.4.

If the diffusion process is considered, there are two possibilities from the point of view of the dopant: (i) doping using solid/liquid sources, and (ii) doping using gas sources. Doping from solid/liquid sources, also called dopant oxide solid source (DOSS) processes, where a liquid doping, normally H₃PO₄ (phosphoric acid) or PCl₃ (phosphorus trichloride), is spin coated on the surface and a phosphorus glass is formed when the samples are introduced in the furnace. In this case, the doping is considered constant and finite, and the obtained profile can be represented by an erfc function.

When doping from gas sources, a carrier with samples is introduced in a hot tubular furnace. Pure nitrogen is used as a carrier gas guided through a container of liquid phosphorus oxychloride (POCl₃) and released to the chamber mixed with oxygen to perform the pre-deposition. This deposited material is a phosphorus silicate glass (PSG) and the flow of POCl₃ is closed [27]. In comparison with the spin on dopant technique, in-line diffusion from gas sources avoids contamination from the ceramic rolls on the conventional furnace, and is the most widely used technique in commercial fabrication lines.
The thermal processes used to diffuse the dopants into the wafer are usually based on the conventional furnace process (CFP) with a temperature around 850°C and times around one hour. However, rapid thermal processes (RTP) are increasing their importance because the diffusion time is reduced to the range of few minutes. In both the CFP and RTP processes, after diffusion and thermal processes, phosphorus glass formed on top of the wafers is etched away by using 10% HF solution.

Over the last decade, research in diffusion processes has been focused in its optimization. Current research in this step (i.e., emitter formation) is focused on producing optimized selective emitters to enhance efficiency. This is discussed in Sec. 2.5.6.

At this point it is also important to mention gettering (absorption) process. After defect reduction in the saw damage etching step, electrically active metallic impurities in the wafer are still present that reduce the lifetime of photogenerated carriers. The thermal processes that diffuse the dopant to form the emitter can also neutralize the electrical activity of some of these impurities by gettering (i.e., absorption of impurities) the locations along the wafer into an inactive energy states, improving the diffusion lengths in the material. This gettering process can also be introduced when Al-based contacts are fired in the fabrication process of the cell. Just as etching is used for the formation of texturing and saw damage etching simultaneously, the formation of the emitter and the firing of Al-based contact are simultaneously used for producing gettering on the electrically active metallic impurities.

2.3.4 Anti-reflection/passivation coating

The c-Si solar cell has two types of losses - optical and electrical losses. Optical losses reduce the quantity of photons that can be absorbed in the Si wafer as they are reflected on the Si surface or on the front side metallic contacts. Also, photons with energy shorter than the bandgap are not absorbed.
Texturization, as discussed above, is one way to reduce optical losses. Another is the deposition of ARC on the front side of the solar cell to enhance the solar radiation absorption and, at the same time, to passivate the c-Si surface. C-Si wafers have an average reflectance between 30% and 40% in the 300-1200 nm range, so an ARC is needed to improve the solar cell. As the quantum efficiency (QE) of Si based solar cell is optimal at 600nm, the refractive indices of air and Si at 600nm are 1 and 3.46, respectively, the ARC refractive index should be around 2 and, consequently, the ARC thickness is around 75nm. For this purpose, Si nitride (SiN) layer is deposited on the Si surface. This step is usually performed by means of a plasma enhanced chemical vapor deposition (PECVD) system by mixing silane (SiH₄), and ammonia (NH₃) in the reaction chamber to form SiN layer on top of Si surface [27]. Improvements in texturization has resulted in a strong focus on SiN as ARC since specific area and the light beam path are different in a pyramidal textured wafers in comparison with non-textured wafers [64].

A surface passivation process consists of the saturation of Si surface bonds to improve and stabilize the electronic properties of the surface. This is used to control and minimize the recombination rate of the charge carriers at the surface, since the charge carrier recombination velocity of an unpassivated surface is very high (around 10⁴-10⁶ cm/s), which decreases the photocurrent.

The SiN anti-reflecting layer acts as effective surface passivation layer for Si surfaces, matching both requirements simultaneously for the fabrication of c-Si based solar cells. As it has been mentioned, this layer is normally deposited using the PECVD technique [65] at a low-temperature of ~300°C. The effects of the bandgap and defects of SiN on carrier lifetime and the transmittance in c-Si solar cells are currently being studied for increasing the values, as the mixing of the precursor gases, flux ratios and temperatures greatly influence the final properties of the solar cell.
Another option is indium tin oxide (ITO). This material is a transparent conductive oxide widely used in solar cell applications. Its optical properties make it an excellent ARC, and its high electrical conductivity allows it to improve the collection efficiency in solar cells. Magnetron sputtering is the common technique used to deposit ITO. A subsequent annealing of the wafer is required to improve the electrical properties of the device. Also, titanium dioxide (TiO₂) has been largely used as ARC in solar cells because the deposition of this material on the Si surface can be performed by atmospheric pressure chemical vapor deposition (APCVD) at low-temperatures. Also, this material is non-toxic, non-corrosive, has a low-cost and shows good surface passivation properties [66]. However, in the 1990s it was replaced by SiN in the standard process because SiN has better surface passivation properties, and can also passivate bulk defects by hydrogenation [23].

SiO₂ grown by thermal oxidation has also been used as ARC and surface passivation layer. However the growth process here is carried out at high temperatures (900-1100°C), making it expensive and incompatible with certain steps that do not withstand those high temperatures. The refractive index of SiO₂ is also not as optimal as SiN for c-Si based solar cells. The amorphous Si oxynitride films observed in the interface between SiO₂/c-Si also introduce recombination traps for carriers that reduce their lifetime. Alternatively, porous Si formed by chemical [67], electrochemical [68] or vapor [57, 69] etching shows impressive properties as ARC. Porous Si in combination with Si oxide (SiOₓ, 0<x<2) can be tuned to the refractive index of the layer. However, the electrical properties of the Si wafer with porous Si layers on the surface traditionally have been very poor for efficient solar cell applications [70]. Hydrogen is the best passivating material for Si surfaces but it is meta-stable. Finally, TiO₂ is an excellent ARC due to its high refractive index of 2.6 at 600 nm, and high transmittance in the range of 300 and 1200 nm. Also, published results are promising because
28

it can be deposited by APCVD offering cost reduction and an easy implementation of this
alternative in the semiconductor industry [71].

### 2.3.5 Metallization

Once the p-n junction has been formed and the ARC deposited on top, the next step is
the metallization on the top and bottom side of the cell. The front side metallization is a grid
composed of busbars (usually two or three), and several thin fingers (70-100 µm wide) that
cover the front side of the cell. The front side metallization produces shadowing losses, series
resistance losses, and determines emitter diffusion profile and surface doping concentration,
and influences the choice of a defined surface passivation technique [72]. For p-type c-Si
wafer, Al is used for back contact and Ag is used for front contact.

A widely used technique to place the metallic contact is screen printing. In the mid-
1970s screen-printed solar cell was first developed [73]. This technique uses a paste, an Al
compound for the back side, and a Ag compound for the front side [74] with micrometric
metal particles and additives. These compounds are pressed to pass through a mesh of steel or
polyvinyl to print the metallic pattern on the Si surface. After the metallic paste is placed, a
firing process is required to produce an Ohmic contact on the Si surface. This technique is
commonly used for in-line c-Si solar cells manufacturing. It is a four step process that
involves: (i) Ag front side metallization and drying, (ii) Ag back side metallization (busbars)
to connect the solar cells into the solar module and another drying process, (iii) back side
blanket Al metallization, and (iv) the firing process, normally between 750°C-850°C [75]. A
complementary option is the finger roller-printing technique. This consists of a rubber wheel
coated with a thin layer of metallization paste that rolls across the wafer for finger contact
[76].

The rear contact also can be placed by physical vapor deposition methods such as
sputtering, thermal or e-beam based evaporation. Using these techniques the formed layers
show very high conductivities. Therefore to reach the performance needed, thinner contact is enough, compared to the screen-printed contacts [27].

One of the most promising techniques [77, 78], normally used with the selective emitter, is the buried contact metallization (Fig. 6). It was commercially applied first by BP Solar in the late 1990s. By means of laser fusion technology, it is possible to make a groove of approximately 20 µm wide and up to 100 µm deep into Si surface. This technique provides two advantages: (i) the reduction of the shadowing loss, from typically 8% from screen printing solar cells to around 3%, and (ii) the filling of the grooves with contact material, reducing around three times the standard width of the metallic, from typically 100 µm in screen printing to 30 µm widths.

Fig. 6 Cross-sectional diagram shows buried contact solar cell. Buried contact solar cell was developed more than 20 years ago and transferred to production line in the early 1990. Laser grooved buried contact solar cell is a high-efficiency commercial technology. Buried contact overcomes disadvantages of screen-printed contacts such as shadowing and series resistance caused by metal grid pattern. To lower shadowing loss and series resistance, metal contact is buried inside the cell with high aspect (height/width) ratio. Using this technology, a narrow strip of closely spaced metal grids can be used on the surface and at the same time high transparency can be maintained. In screen-printed solar cells, 5-7% of incoming light is blocked due to shadowing, whereas in buried contact solar cells, metal lines can be less than 20 µm and this corresponds to <3.5% shadowing. Lower shadowing loss results less reflection from the surface, and improvement in $J_{sc}$. 

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The main reasons that the buried contact metallization has not been further introduced in the industrial process for manufacturing solar cells are that this technique produces defects on the Si surface, leading to decrease in cell performance and increase in the production cost. Consequently, these drawbacks need to be overcome for the buried contact metallization to surpass screen printing as the preferred technology for metallic contacts of Si solar cells.

Currently, standard metals used for the front side and back side metallization are Ag and Al, respectively. However other less expensive alternatives for the front side, such as copper (Cu), has been studied for more than 10 years [79] to replace Ag. A recent work [80] analyzes the current and future front side metallization scenario, suggesting that the metallization with Ag is expected to be reduced in the coming next 10 years, decreasing from the current 90% to a 50% of the market share. Simultaneously Cu and other alternative materials will increase their relevance as substitutes of Ag. An important reason why one metal may replace another over the years when it comes to solar cells is global demand-and-supply of various metals.

### 2.4 Other types of c-Si based solar cells

Some of the solar cells discussed in this section are very expensive compared to the ones obtained by the standard procedure described in Sec. 2.3 and commonly used in the industry. However as research into these solar cells continues, a subsequent reduction in production costs may be expected. At the same time, some of the features of these solar cells may be incorporated to current commercial standard procedures and result in efficiency and cost improvements.

As reported [81], advanced solar cells such as PERC, bifacial solar cells (light sensitive on both sides) and n-type solar cells have gained relatively considerable attention. In the PERC structure, as shown in Fig. 7, full area Al-BSF is replaced by a dielectric passivation, which is locally opened for the placement of the metallic contact [82]. 21.2%
efficiency is the highest value reported so far [83]. Rear side dielectric passivation layer(s) improve passivation quality and internal reflection compared to full area Al-BSF.

Fig. 7 Schematic diagram shows cross-section of PERC solar cell structure. The rear side of PERC cell is passivated by dielectric/stack except at the region where contact metal is touching c-Si. Rear side dielectric (oxide) acts as mirror, reflects light into the bulk and thereby improving photocurrent. A major advantage of using rear side passivation instead of full area Al-BSF is the enhancement in $J_{sc}$ that comes from enhanced reflectivity of 90-95% at 1000 nm compared to 65% from full area Al-BSF [84]. By reducing metallization fraction at the rear side, defects at metal/c-Si interface becomes less effective and the difference in $V_{oc}$ and $J_{sc}$ between PERC and PERL cells becomes small. When thinner c-Si is used for fabrication, reflectivity from rear structure becomes significant. PERC technology developed by Roth & Rau and successfully implemented under the name MB-PERC.

In other words, compared to full area Al-BSF cell, PERC advantages are lower SRV and an improved optical performance. However, additional reduction of the SRV and optimal use of high-resistivity materials can be performed in the PERL cell structure, which has at present 1 sun world efficiency record of 25% for c-Si based solar cells since 1998. PERL type bifacial structures have also been introduced in the industrial production lines over the last 5 years, substituting the inverted pyramids by chemically formed pyramids. Cross-sectional diagram of PERL cell is shown in Fig. 8. Advantages and disadvantages of local BSF are discussed in Sec.2.5.7.
Fig. 8 Schematic diagram shows PERL solar cell structure. In the inverted pyramid surface, incident light undergoes double bounces meaning that incident light will have two chances of transmission into c-Si. In PERL structure, at the rear side, to reduce minority-carrier recombination at the metal/c-Si interface, boron diffusion is performed locally under the metal contact, whereas in PERC structure local diffusion is not performed under the metal contact. Local BSF in PERL cell improves $V_{oc}$ and $J_{sc}$ since electric field in the BSF region between $p^+/p$ junction drives electrons away towards the $p-n$ junction and reduces surface recombination at the defective metal/c-Si interface. PERL cell technology named as Pluto was developed by Martin Green and Stuart Wenham at University of New South Wales and commercialized by Suntech Power.

The MWT solar cell is a back contact solar cell that uses a technology very similar to that of conventional screen-printed solar cells. MWT solar cell is shown in Fig. 9. As compared to conventional solar cell technology, only two additional steps are required, viz. (i) via drilling for the interconnection between front and back side, and (ii) the metallization through vias (holes). An efficiency gain of about 0.5% in absolute terms and a current gain of about 3.5% due to less shading on the front side are achieved as compared to the standard cell concept [85]. A highest average and peak efficiency of 19.6% and 20.0% has been reported for MWT c-Si solar cells [86].
Fig. 9 (a) Schematic diagram of MWT solar cell [87], and (b) top view showing front finger grids and absence of busbars [88]. On the rear side busbars are wide and therefore, series resistance loss arising due to busbar can be eliminated. MWT cells have higher efficiency (~0.5%) than conventional solar cells due 50% less shading/metallization area on the front side [89, 90]. Less shadowing improves $J_{sc}$ and fill factor. MWT c-Si solar cell technology has been transferred successfully to production [86, 91] and the cells have produced an average and peak efficiency of 19.6% and 20.0% respectively. For MWT cells, welding is not required when assembling MWT cells into modules and results in lower power loss and lower cell breakage rate. Fig. 9 (b) from [88], Tobias Fellmeth, Michael Menkoe, Florian Clement, Daniel Biro, Ralf Preu, Highly efficient industrially feasible metal wrap through (MWT) Si solar cells, Solar Energy Materials & Solar Cells 94 (2010) 1996–2001. © Elsevier 2010. License number 3457011111677.

The EWT solar cells are similar to the MWT solar cells. The difference lies in the fact that here the n-type contacts are placed on the rear side. The rear surface of the wafer presents an emitter structure that is connected through with the front surface emitter. EWT solar cell is shown in Fig. 10.

The emitters on the front and rear side can both collect charge carriers. This makes the EWT cell very attractive for low lifetime materials. However this structure presents a series resistance problem [27]. Moreover expensive metallic formation techniques are required. The lack of significant current research focus on EWT, as gauged through the paucity of research publications per year, suggests that the future of EWT solar cells is uncertain.
Fig. 10 Picture shows EWT solar cell structure [92] quite similar to back contact back junction solar cell. Laser drilling is used to open 15000 vias (holes) having each 80µm diameter. Several thousands of vias/sec can be drilled [93]. In EWT cell, no grids lines, and no busbars are present on the light entering side (note that in MWT structure, grid lines are present on the light entering side, and no busbar is present). Both p-type and n-type grids as well as busbars are placed on the rear side, and trade-off between shadowing loss and series resistance is eliminated. Grid less front surface enhances light incident area and improves $J_{sc}$, fill factor since on the rear side grid lines and busbars can be wide. Reproduced from [92], James M. Gee, Prabhat Kumar, James Howarth, Todd Schroeder, Jeff Franklin, Jason Dominguez and David Tanner, Development of industrial high-efficiency back-contact czochralski-Si solar cells, Prog. Photovolt: Res. Appl. 19 (2011) 887. © Copyright 2011 John Wiley & Sons, Ltd. License number 3457020769998.

Another interesting area of current research is the realization of bifacial solar cell with boron diffusion either from a gas source or a solid source such as a boron silicate glass. A conversion efficiency of 18.4% has been obtained on c-Si wafers using boron BSF and Si carbide (SiC)/SiN ARCs. This structure easily fits with the development of a selective emitter at the front side of the cell and can potentially achieve conversion efficiencies above 19% [94].

2.5 Low-cost c-Si based solar cells

Since cost and efficiency of solar cells are the most important determining factors for commercial utilization, it is worthwhile to further explore how these issues are being currently addressed. In the context of solar cell development, low-cost always refers to cost per unit of energy or power, being the figure of merit $$/Wp preferred to that of $$/kWh due to the fact that the former focuses on technology and discards the influence of radiation, system
reliability and other factors. Lowering the cost means minimizing the $/Wp, and to fulfill this
goal, two approaches can be followed: reduce the numerator (so, looking for cheaper
processes) or increase the denominator (so, producing more efficient cells), or both.

To lower the cost of c-Si solar cell, the following routes are pursued: use of lower
quality Si feedstock and wafers, search for cheaper dopant sources, and search for cheaper
metallization schemes. To increase the efficiency, the efforts in the field of front junction
solar cells have been focused in implementing selective emitters at the front and reducing
BSF recombination at the rear by industrially feasible processes. All these concepts are
reviewed in the following sections.

2.5.1 Low-cost Si wafers: Relaxing feedstock specifications

The raw material for Si solar cells has traditionally come from the polysilicon market
for microelectronics, providing a ultrapure feedstock at a cost that accounts for around 15%-20% of the total PV module cost (in $/Wp). The availability of Si due to the tremendous
growth of the PV sector and the search for cheaper purification routes have motivated
research into alternatives to the traditional so-called Siemens process. As mentioned in Sec.
2.2.1, in this process, metallurgical Si is transformed into a volatile compound, typically
TCS, which is further purified and then converted back to solid Si in a chemical vapor
deposition process. Some of the alternatives rely on the same basis, but introduce significant
changes in certain steps of the process. For example, using SiH$_4$ as the intermediate volatile
compound produces Si deposition in a fluidized bed reactor or a free space reactor [95]. Their
promoters claim that the quality of the resulting material is similar to the conventional one, so
no further adaptation of the solar cell process is needed. Recycling the byproducts efficiently
is also an option.

Another group of alternatives avoids the conversion of metallurgical Si into a volatile
compound, and upgrade the metallurgical Si through a combination of steps suited for
different impurities [96,97], decreasing to some extent the energy consumption in the
deposition step and hence the cost of the process. The purity usually reached with these
processes is lower than that of the TCS route, but that does not necessarily mean that the
material cannot be used for solar cells. In fact, by introducing some changes in the thermal
profiles of the crystallization and solar cell processing steps, similar solar cell efficiencies
have been achieved with this material to the semiconductor grade one [98-101].

At a broader level, though, a drastic reduction in cost of conventional polysilicon is
hindering the development of these alternatives. In order to be commercially viable, there is a
need to clearly justify their good performance versus satisfactory yield and cost-effectiveness
in order to undertake the large investments with the production.

### 2.5.2 Producing cheaper wafers

Si wafers for solar cells are made by slicing ingots grown by either monocrystalline
technique or the multicrystalline one. Recently, a new crystallization process has been
proposed that aims to combine the high-throughput of the latter with the better quality of the
former. This is done through the use of monocrystalline seeds on the bottom of the crucible in
a directional solidification furnace [102]. It has been called mono-like or quasi-mono, due to
the fact that the ingot is not 100% monocrystalline, as crystals of different orientations
nucleate from the walls of the crucible. Figure 11 depicts an example of wafer-type
distribution. Even though efficiency increases of 1-1.5% in absolute have been reported
compared to traditional casting, to fully exploit the potential of the material a few issues
should be industrially addressed: the need of sample classification to apply different solar cell
process conditions to different samples (which comes for example from the different
texturing techniques applied to mono and multi wafers), and the fact that part of the material,
even the monocrystalline one, is rich in dislocations [103-105].
Fig. 11 Wafer-type distribution of a mono-like ingot according to their percentage of macroscopic monocrystalline feature: MC: mono-casting (100% mono); QM: quasimono (>90% mono); DCW+: DC Wafers PLUS (>75% mono); MULTI: mono/multi and mc-Si (<75% mono). With permission from [105], Ismael Guerrero, Vicente Parra, Teresa Carballo, Andrés Black, Miguel Miranda, David Cancelli, Benito Moralejo, Juan Jiménez, Jean-François Lelièvre, Carlos Cañizo, About the origin of low wafer performance and crystal defect generation on seed-cast growth of industrial mono-like Si ingots, Prog. Photov: Res. Appl. 22 (2012) 923. Copyright © 2012 John Wiley & Sons, Ltd. License number 3457490569073.

Another approach that offers the advantage of eliminating the slicing process is the growth of thin Si ribbons directly from a polysilicon melt. Several technologies, such as edge defined film-fed growth, string ribbon, dendritic web (WEB, recently revisited as Ribbon on a Sacrificial Template), and ribbon growth on wafer has been promoted [106]. Industrial efficiencies in the range of 15-16% have been reached by the most advanced techniques, while others are on the 13-14% level [107-109]. With more sophisticated processing, efficiencies around 18% have been reached [110,111]. Although their cost reduction potential remains, there are also other current market conditions that are slowing their development. The drawback of all of them is the high density of defects (dislocations, grain boundaries, impurities) and the uneven surfaces that require specific processes for texturing, phosphorus diffusion, SiN) deposition or screen printing for implementing in the solar cell process. These
processes may even need replacement with alternative techniques, for example, the direct writing of Ag pastes for metallization [112,113].

2.5.3 Living with defects and impurities

Solar cell processing should integrate steps that can reduce the deleterious effect of impurities and crystalline defects. These steps are gathered under the concept of defect engineering. In fact, solar cells made of traditional Si sources already benefit from them, in particular from external gettering of impurities to the phosphorous and Al layers, as we explained in Sec. 2.3.3. In wafers from low-cost sources, or even in those coming from the border and edge regions of multicrystalline ingots where the density of impurities is higher due to in-diffusion from the crucible, defect engineering techniques aim at manipulating metal concentrations and distributions to reduce their impact in solar cell performance [114]. For example, it has been shown that a slow cool down or a low-temperature plateau after phosphorous diffusion reduces iron (Fe) interstitials, and increases carrier lifetime and solar cell efficiency [115-117]. Other strategies such as implementing thermal pretreatments or changing the firing step thermal profiles are being studied [118-120]. As an example taken from Ref. [119], Fig. 12 compares the effect of a standard firing step (realized in this case in a RTP furnace), which produces an increase in interstitial Fe concentration due to precipitate dissolution. On the other hand, with a modified one (which is called extended RTP) segregation gettering is enhanced and so contamination levels are reduced.
The challenge here is to implement defect engineering techniques at the industrial level, where modifying thermal step profiles can impact throughput, and where tailoring processes to specific wafers introduces further complexity.

2.5.4 Low-cost approaches for doping

Emitter doping from a POCl$_3$ liquid source in a quartz furnace has the drawback of being a batch type process, and in-line options are promoted, where a phosphorus source is applied to the wafer surface, dried, and then diffused in an infra-red belt furnace, benefiting from automation, high-throughput and the ability to implement temperature profiles. Dopant sources can be screen-printed [121], spun-on [122-126], sprayed-on [127-130], deposited by CVD [131] or even diffused from a gas source [132]. In some of the reported experiments, dopant drive-in is performed by RTP and not in an infrared furnace.
Efforts in characterizing emitter performance have been successfully applied, in terms of dopant diffusion, sheet resistance and emitter saturation current. An example of the comparison of the saturation current with state-of-the-art POCl₃ diffusion is given in Fig.13, taken from Ref. [131].

Fig. 13 Emitter saturation current densities (represents sum of all recombination currents in the emitter), obtained from lifetime measurements, of passivated samples doped by the method proposed on [127] before and after firing. Values for two different diffusion processes (Diff-65 and Diff-75) and two different oxidation processes (DCE-850 and Dry-900) are given. The values are under those of a typical POCl₃ process (which is marked with stars with the number 0). Reproduced with permission from [131], Fallisch A, Wagenmann D, Keding R, Trogus D, Hofmann M, Rentsch J, Reinecke H, Biro D., Analysis of Phosphorus-Doped Si Oxide Layers Deposited by Means of PECVD as a Dopant Source in Diffusion Processes. IEEE J. Photovoltaics, 2 (2012) 450. Copyright © 2012 IEEE. License number 3504480294880.

Solutions currently exist that take advantage of these low-cost doping technologies, addressing key aspects such as emitter homogeneity, lack of shunting and gettering ability, and successful implementation of emitter profiles with convenient sheet resistances. Furthermore, some of these approaches have the potential to achieve high-efficiencies, with efficiencies of 18%-19% being reported for c-Si [125,126] and 15%-16% for mc-Si [123,133] based solar cells.
Boron, as a p-type dopant can substitute Al in BSF layers, reducing recombination and bowing, and can also form the p-n junction on n-type c-Si wafers. Cost-effective techniques to diffuse boron are being promoted [134-136], as the traditional boron tribromide (BBr₃) source in a diffusion furnace implies a batch type process, and a somewhat involved process optimization [137,138]. The use of these alternative dopant sources can also facilitate the implementation of local BSFs. Passivation of boron doped layers is also an aspect that needs specific solutions [139].

Finally, ion implantation is another option, for both phosphorus and boron doping [140,141] that benefits from its wide use in microelectronics. Ion implantation allows for an accurate control of the dose and depth of the dopant, and needs a subsequent annealing to reduce the damage introduced by the implantation.

2.5.5 Low-cost approaches for metallization

Traditional screen printing metallization is evolving towards lower consumption of expensive Ag, thinner fingers to improve the aspect ratio (height/width), and different paste formulation to contact lowly doped emitters. Substituting mesh screens by stencil-based screens may help to reach finer lines (50-60 µm) with better aspect ratios, and benefit from a slower deterioration of the printed patterns [142]. Separating screen printing for fingers and busbars (which is called dual printing) may help in optimizing separately geometry and paste formulation [143].
Another approach that is compatible with the use of stencil screens or the dual printing is to separate metal deposition in two steps: first a layer designed for good contact with Si is deposited, which is followed by a second layer designed to increase conductivity. The simplest would be to optimize the properties of two different pastes that are being used in industry as double printing or print-on-print [144,145]. Alternatively, the contact layer can be done by roller printing [146], pad printing [147] or nickel plating [148]. Inkjet printing is also being explored, as it can produce thin lines and as a non-contact method it can avoid mechanical problems with very thin wafers [149]. To overcome limitations in metal particle sizes that may obstruct the printer, an aerosol technique can be implemented instead [150].
For thickening of the layer, light-induced electroplating is a good candidate that can give very favorable aspect ratios [151]. Examples of techniques resulting in improved finger cross sections are shown in Fig.14. The challenge in all these cases is to implement the techniques at the industrial level with sufficient throughput and reproducibility [152].

**2.5.6 Efficiency enhancement: Industrially feasible selective emitter technologies**

A selective emitter [153] is formed by heavily doping underneath the contact grid and by weakly doping the illuminated area (Fig.15). This doping also results in an adequate sheet resistance to improve the electrical properties of the front metallic contact and low resistance in the illuminated areas.

Fig. 15 Schematic diagram shows the location of the selective emitter having a low sheet resistance of 35-55 Ω/square. A selective emitter is a front junction, front contact solar cell configuration. Using this approach, in selective regions, i.e. surface regions underneath the grids are heavily doped to improve electrical (ohmic) contact between the grid and Si. The remaining emitter surface regions between the grids are lightly doped to minimize recombination losses and to improve cell’s blue response. In other words, selective emitter structure is used to reduce losses originating from the front side. Selective emitter can be formed by laser doping, doped Ag paste, screen printing, etchback etc.

The optimum emitter profile is different for a contacted region than for a passivated non-contacted one (with higher surface concentration and longer junction depth in the first case). While in traditional cells a design compromise is reached, resulting in emitters of 50-75 Ω/square, the process here can implement selective emitters, provided the gain in
efficiency justifies the increase in complexity. While selective emitters have been
implemented in laboratory cells since long ago [154], recent efforts have succeeded in
adapting the concept to an industrial environment through the use of a number of techniques
[153].

(i) Performing two separate diffusions, a heavier one restricted to the regions to be metallized
by a screen-printed or deposited by mask [155].

(ii) First diffusing a homogeneous thick emitter by conventional means; then applying a
screen-printed or inkjet mask to protect the regions to be metallized, and removing the
superficial dead layer in the non-protected region by a plasma etch [156], a wet etch [157] or
an etching paste [158].

(iii) Diffusing a solid dopant in the areas to be contacted, so that a highly doped emitter is
formed there, while a much lighter diffusion takes place at the uncovered regions from the
gas phase [159].

(iv) Protecting the regions that will not be contacted with a mask, so that during phosphorous
diffusion a highly doped emitter is formed in the non-protected areas, while under the
protected ones only a smaller dose of dopant is able to diffuse into the Si because the mask
slows down penetration, giving thus a low doped emitter there. The mask is subsequently
removed [160].

(v) Forming first a high sheet resistance emitter, and then screen printing a metallization
paste containing phosphorus, so that when firing, a heavily doped alloyed layer is formed
under the metal fingers [161]. The drive-in of the heavier doped region can also be done by
laser [162].

Most of these techniques require some kind of pattern aligning to print the front contact
fingers on the heavily-doped regions, something suitable for state-of-the-art automatic
equipment. Gains in absolute efficiency of around 0.5% have been reported.
2.5.7 Local BSF at the rear: Advantages and drawbacks of the technologies implemented in industry

Passivating the rear surface with a dielectric film can increase cell efficiency, especially for wafers were carrier diffusion length is higher than thickness. Rear side recombination can be reduced as compared to a full BSF, and good reflecting properties can be achieved, provided the Si surface morphology is adequately prepared [163]. The rear metal contact can be implemented locally, in dots or lines, together with a BSF, or without it. In the second case, attention should be paid so that contact resistance is maintained in reasonable levels.

Since this concept has been implemented to produce high-efficiency laboratory solar cells [164], efforts have been made to transfer this technology to industry, with the focus on throughput. Layers such as SiO₅ [165], Al oxide [166], Si oxynitride [167] and SiC [168] are the best potential candidates. A-Si:H has been also applied as rear side passivating layer [169], but its full potential is exploited in the heterojunction structure, as discussed in Sec.4.

Care must be taken with the potential loss of passivation due to the subsequent metallization, as high-temperature steps can degrade the passivating properties of the layers [170,171]. Another issue is the possibility of shunting by interaction between the layer and the metallization due to the existence of charges in the layer, as is the case of SiN layers [172].

With proper process optimization, or by combining several layers in stacks, the low effective rear surface recombination velocities, in the range of few cm/s, have been successfully obtained in solar cells to improve efficiency [173-177]. A clear proof of the gain obtained with the rear surface passivation can be seen in the internal quantum efficiency (IQE) curve in an example taken from Ref. [145], and shown in Fig. 2.16.
Fig. 16 Comparison of internal quantum efficiency and reflectance between cells with different rear passivation stacks, $\text{Al}_2\text{O}_3/\text{SiN}$ and $\text{SiO}_2/\text{SiN}$, as compared to a full-area Al-BSF reference cell [145]. With permission from Thorsten Dullweber, Sebastian Gatz, Helge Hannebauer, Tom Falcon, Rene Hesse, Jan Schmidt, Rolf Brendel, Towards 20% efficient large-area screen-printed rear-passivated Si solar cells, Prog. in Photov: Res. Appl., 20 (2011) 630. Copyright © 2011 John Wiley & Sons, Ltd. License number 3457590457465.

2.6 Future outlook

Efficiency of traditional c-Si solar cells has increased relatively significantly since their invention in the mid-twentieth century. To a great extent this has been due to several improvements related to larger photon and charge carrier collection, improved photoconversion processes, and shadowing reduction, as has been mentioned in previous sections. Consequently, the current efficiency for commercial c-Si solar cells is quite close to the world records obtained in lab. Due to the mass scale adaption of laboratory techniques in the industry, such as buried contacts, selective emitters, etc., in recent years the cost of these new techniques has been lowered sharply. One of the most important challenges of the c-Si technology is to increase short-circuit current density ($J_{sc}$), using low-cost manufacturing processes. Currently, the results obtained applying the RIE process are very promising, and its inclusion in the commercial production lines may be explored in to increase the $J_{sc}$ values. Other improvements, such as the introduction of back reflectors, can be implemented with the current state-of-art of the metallization techniques such as evaporation. The main challenge
for this technique is to become as cost-competitive as screen printing. Multilayers are also an attractive option for improving the $J_{sc}$ values, especially as the price of the PECVD systems dropped in recent years. In order to improve the open-circuit voltage ($V_{oc}$) of the solar cells, ion implantation is one of the most interesting techniques to obtain more repeatable profiles. Also, it is possible to obtain higher accuracy in the doping profile, and also improve the current selective emitter formation procedure. However, due to Si material properties, $V_{oc}$ for a single-junction solar cell is now very close to the theoretical limit. Further incremental improvements in $V_{oc}$ require investments in sophisticated fabrication/manufacturing techniques, which will increase the cost. Finally, to reduce shadowing losses new pastes and materials have been tested in laboratories in recent years, which show remarkable results in terms of electrical performance improvements. Consequently, in the next 5 years narrower and thinner metallic contacts in the solar cells will be commercially applied to c-Si solar cells. These new materials will reduce shadowing and, at the same time, result in low series resistance. On a side note, the main challenge in solar cell is to reduce surface/bulk defects to achieve low emitter saturation current density.

Conventional front junction cells also continue to make rapid advances. Many alternatives to front junction solar cells with front and rear contacts are being promoted, and the traditional structure has demonstrated strong potential to reduce costs. Over the last several years, impressive improvements have been achieved thanks to a successful transfer to industry of some of the concepts being pursued by the research community. These have included the use of lower cost feedstock, cheaper ingots and wafers, development of low-cost dopant and metallization schemes, and implementation of selective emitters and rear passivating stacks. These achievements have brought the cost of c-Si PV modules well below $1/Wp$ (excluding balance of systems), a reduction of around 75% in ten years. There is however still room for further improvement of front junction solar cells towards the
$0.50/Wp$ range, thanks to technology improvements and economies of scale. In a tough competitive environment, those concepts combining the lowest costs with the highest improvements in efficiency will become dominant.

**3.0 c-Si based solar cells: Back junction**

The major advantage of the interdigitated back contact (IBC) c-Si solar cells is the absence of front side metallization grid, since both p-type and n-type metal electrodes for emitter and base respectively are located on the rear side of the solar cell. Due to the absence of front side metallization grid, IBC cells exhibit zero-shading losses, which results in strongly increased $J_{sc}$. Moreover, the front surface can be optimized for optimum light trapping and surface passivation properties, without having to allow for the low contact resistance. This way the front surface recombination can be reduced and light trapping improved. Furthermore, the series resistance losses of the metallization grid can be reduced, because both electrodes are on the back side where the width and thickness of the metallization grid is not limited by the shading losses. All of these positive effects result in a relatively very high-efficiency potential of this type of c-Si solar cell.

**3.1 Introduction**

The schematic diagram of IBC back junction solar cell is shown in Fig. 17. A remarkable example of the high-efficiency potential of this cell structure are the IBC cells developed by the SunPower Corp., with the highest reported efficiency for the large-area (155.1 cm$^2$ n-type Cz c-Si) IBC solar cell of 24.2% [178], and module based on IBC cells with efficiency over 20% [179]. The decrease in module efficiency is attributed to the fact that (i) the module area is not fully covered with solar cells (i.e. there is inactive area), (ii) the encapsulation foils and glass sheet in module introduce additional optical losses, and (iii) finally the interconnections of the individual solar cells in the PV modules cause some resistive losses.
The IBC cell structure also offers advantages for the module manufacturing. Both electrodes on the rear side allow for the potentially easier and fully automated co-planar interconnection of the back-contact solar cells in the module assembly process. The issue of the module technology for the interconnection of the IBC cells is under investigation and should allow for further reduction of the PV modules based on the IBC cells structure [180-182]. Also, the attractive and uniform appearance of the finished IBC modules should be noted, as it is especially of importance in the field of building integrated photovoltaics (BIPV).

The operating principle of the IBC c-Si solar cell is shown in Fig. 17 (a), and the examples of the photographs of the IBC solar cells are shown in Fig. 18. The incoming photons generate electron-hole pairs. Most of the absorption takes place close to the front surface of the IBC solar cell, resulting in a charge carrier (electrons and holes) concentration gradient through the c-Si bulk. The concentration gradient of the carriers results in the diffusion transport towards the rear side, where the p-n junction is located and carriers are collected by their respective electrodes. The p-n junction on the rear side may have a point-like structure, or a line structure with the respective width. The distance between two metal contacts of the same polarity is called pitch.

![Fig. 17 (a) Schematic cross-section of an n-type high-efficiency IBC c-Si solar cell having p-n junction at the rear side, (b) schematic angle view of the IBC cell introduced by Lammert and Schwartz [183]. To avoid minority-carrier recombination at the rear side and to enhance the minority-carrier collection probability, emitter size is kept larger than the BSF size. Front surface field blocks minority carriers reaching the front surface. The...](image-url)
Historically, the concept of the IBC cells was introduced in 1977 by Lammert and Schwartz. Initially the IBC cells were developed for the operation under high level of sunlight concentration. The research group led by R. Swanson at Stanford University and at the SunPower Corp., founded by R. Swanson paved the way for the remarkable development of IBC cell physics, design, and technology [178,179,185-190]. Currently many research groups and industrial laboratories are investigating the IBC cell concept due to its inherent high-efficiency potential, with the goal to reduce the costs of the c-Si PV modules.

The other two categories of the c-Si back contact solar cells are the MWT cells [191-193], in which the front surface collecting junction and the front metallization grid are connected to the interconnection pads on the back surface via laser-drilled holes (Fig. 9), and the EWT cells [194-198], in which the front surface collecting junction is connected to the interdigitated contacts on the back surface via laser-drilled holes (Fig. 10). The MWT and EWT cell structures are covered in Sec. 2.4. The interested reader is referred to [199] and to the above listed references for more details.
3.2 Challenges related to c-Si back junction solar cells

One of the main challenges to the spread of IBC solar cells into mass production is the complexity of the processing technology. Processing of major rear side features of IBC cells such as: (i) emitter and BSF doping areas, (ii) contact openings in the passivation layer, and (iii) the metallization grid, requires four to six masking steps. Laboratory development usually includes application of the photolithography process, as shown in Fig.19, for structuring of the rear side of the IBC cells.
Texturization and n+ BSF diffusion (phosphorus diffusion)

Oxide removal

Masking oxide growth

Photoresist deposition

Oxide etch and Photoresist removal

Texturization and n+ BSF diffusion (phosphorus diffusion)

Legend

- n-type Si wafer
- Silicon oxide
- N+ phosphorus doped region
- P+ boron doped region
- Metallization
- Photoresist

Fig. 19 Possible example of a complex laboratory scale process flow for the IBC solar cell processing using photolithography and high-temperature diffusion processes. The sequence for fabrication is first the left column and later the right column. Highly pure, lightly doped Fz c-Si wafers with diffusion length at least 4 times higher than the wafer thickness, and life-time of 1-3 msec are required. High accuracy masking steps are required to avoid shunting between p-type and n-type electrodes. Instead of expensive photolithography process, laser processing and screen-printing are used to obtain high-throughput.

Photolithography is however not a cost-effective process for mass production in the photovoltaic industry. The processing sequence of the IBC cells is therefore much more complex than conventional c-Si solar cells, which results in increased manufacturing costs. There exists the need for simplified processing schemes, where costly photolithography process is replaced with low-cost and high-throughput structuring schemes using laser processing and screen-printing, etc. However since there exists a risk of fatal shunting between the p- and n-type electrodes due to errors in the masking processes, requirements of high positioning accuracy and resolution are imposed on the masking steps. In addition to the complexity of the processing technology, IBC require high quality of c-Si wafer and the high-quality passivation of the wafer surfaces.

The above issues of processing complexity and c-Si material requirements are of major importance and are therefore discussed in detail in the following sections.

3.3 Requirements for front surface passivation and bulk minority-carrier lifetime
Due to absorption properties of c-Si, most of the photogeneration occurs at the front side of the cell (Fig. 17a). At the same time, in the IBC cell structure, the collecting p-n junction is located on the back side. Due to concentration gradient across the bulk, photogenerated charge carriers travel from front side to rear side and are collected by their respective electrodes. For poorly passivated front surface, photogenerated minority-carriers can be easily lost by recombining at the front surface instead of reaching the back junction. Moreover, even if the front surface is well passivated, a risk of recombination within the bulk c-Si exists. The carriers which need to diffuse through the wafer thickness can recombine in bulk c-Si before reaching the back junction if the bulk lifetime of the minority-carriers is insufficient. Therefore, minority-carrier lifetime in bulk ($\tau_{\text{bulk}}$) and front SRV are the two most critical parameters in the IBC solar cell structure. The importance of these two critical parameters is shown in Fig. 20. The starting Si material needs to be of high quality (the minority-carrier lifetime should be in the range of 1-3ms) and its quality needs to be maintained during the whole solar cell processing sequence in order to reach high-efficiencies. The rule-of-thumb is that the diffusion length of the minority-carriers in c-Si needs to be at least four times higher than the thickness of the c-Si wafer in the IBC solar cells, to allow for efficiencies above 21-22%. This means that $\tau_{\text{bulk}}$ needs to be in the range of milliseconds. Simultaneously the front SRV needs to be kept extremely low in the finished device in order to enable high-efficiencies. The effective front SRV should be kept below 10cm/s.
Fig. 20 Example of numerical simulations of the efficiency of a back junction solar cell structure as a function of bulk life-time and front surface recombination velocity. Front surface recombination velocity and diffusion length of minority-carriers are the ultimate parameters controlling the efficiency. For high-efficiency, effective front surface recombination velocity should be less than 10 cm/s. Simulations were done using PC1D [200] program (graph adopted from [184]). From [184], F. Granek, Ph.D thesis, “High-efficiency Back-Contact Back-Junction Silicon Solar Cells”, Verlag Dr. Hut, ISBN 978-3-86853-348-4 (2009). Permission granted.

3.3.1 Minority-carrier lifetime considerations

The extremely high requirements for the minority-carrier lifetime can be in practice met only by an n-type Si as base material. In p-type boron-doped oxygen-contaminated c-Si, minority-carrier lifetime is strongly reduced under illumination or carrier injection [201, 202]. Due to the lack of boron in n-type Si, no degradation occurs. Also, n-type c-Si exhibits lower sensitivity to the impurities as interstitial Fe [203]. Many laboratories are developing front junction and rear junction solar cells based on n-type c-Si [137, 204-209], and commercially available solar cells with the highest-efficiency are produced on n-type c-Si wafers [178]. The drive for low-cost in the PV world requires however that the Si wafers need to be manufactured using industrially relevant manufacturing methods. In reality only phosphorus doped n-type wafers cut from Cz-grown ingots meet these requirements [28, 210]. The lifetime of the minority-carriers in n-type c-Si is significantly higher than in the case of p-type c-Si. For example, extremely high minority-carrier lifetime in the range of milliseconds was reported for n-type mc-Si by Cuevas et al. [211].

3.3.2 Front surface passivation considerations
High quality of front surface passivation can be achieved by the application of dielectric passivation layers such a thin thermal SiO$_2$ layer covered by the PECVD SiN ARCs [212]. However, the front surface passivation is usually additionally improved by the additional phosphorus doping layer on the front side. This is called front surface field (FSF) and its role is to reduce the concentration of the minority charge carrier close to the wafer surface, and thus reduce the effective recombination velocity [213,214]. The methodology for numerical optimization of the doping profile of the FSF for the passivation purposes was presented by del Alamo and Swanson [215]. The application of the FSF has also additional important positive impacts on the IBC cell performance. FSF improves long-term stability of the front surface passivation under UV illumination [212]. It also improves the current linearity of the IBC cells at low light intensities, thus improving the efficiency at the low-illumination intensities [216]. An FSF layer is also seen to significantly improve lateral current transport by reducing the lateral base series resistance losses [217].

3.4 Approaches to minimize losses related to the rear side structure

The next main challenge in achieving very high conversion efficiencies in IBC cells is in the rear side structure. Introduction of the complex doping grid of the interdigitated emitter and base areas on the rear side is not only technologically challenging, but also accompanies some additional risks to achieving high-efficiencies. The recent study of Kluska et al. [218] investigates systematically the loss mechanisms on the high-efficiency IBC solar cells. Next to the front surface and bulk recombination of the minority-carriers, this study describes free carrier absorption and electrical shading as the critical loss mechanisms.

In the free carrier absorption process [219,220], the incident photon’s energy is absorbed by free carriers. This is a parasitic absorption (optical absorption that does not produce e-h pair is known as parasitic absorption) process, leading to a reduction of the
photogenerated current. The free carrier absorption process is significant only in the highly
doped c-Si wafers. A careful optimization of the doping profiles of the emitter and BSF
regions is therefore a must when reducing the free carrier absorption losses and at the same
time minimizing the rear surface recombination losses [221].

Electrical shading losses are recombination losses of the minority-carriers at the rear
side areas not covered by the emitter (shown schematically in Fig. 21). Electrical shading
losses have a significant impact on the efficiency of the IBC solar cells. Therefore careful
optimization of the rear side geometry, doping profiles, and rear surface passivation quality
are crucial in order to achieve high-efficiency [221-224].

Fig. 21 Sketch of the (i) rear side, and (ii) light beam induced current (LBIC) map of the laboratory scale
(2x2cm²) IBC c-Si solar cell. The reduced signals above the base fingers and the base busbar due to electrical
shading are clearly visible [222]. Here, (a) and (b) refers to base finger and base busbar. Cell efficiency is
affected by electrical shading (losses) at the rear side. Doping profile and pitch size at the rear side should be
optimized for high-efficiency. With permission from [222], M. Hermle, F. Granek, O. Schultz-Wittmann, S. W.
3582490239489.

In order to reduce the electrical shading losses, other approaches emerged recently to
drastically reduce the rear side surface related losses apart from the optimization of the rear
side emitter and BSF doping profiles in the classical IBC cell structure. These approaches are
based on decoupling the geometries for the minority-carrier collection and metallization.
They should allow for nearly complete elimination of the electrical shading losses. A
prominent example of such approaches include buried emitter IBC solar cell [221, 225, 226],
which introduces a local overcompensation of the emitter by the BSF doping and drastically improves the emitter coverage on the rear side seen from the front surface side (see Fig. 22 for explanation of the buried emitter structure). Another example involves decoupling emitter from metallization geometry by the application of the insulating thin-films, which can lead to efficiencies up to 23% [227,228].

Fig. 22 Cross sectional view of the buried emitter back junction solar cell. When looking from the top of the solar cell, the boron emitter is extended over almost the entire rear side of the solar cell. This allows for efficient collection of minority-carriers at the rear side. At the same time the emitter regions are electrically insulated from the base metallization by BSF layer, which prevents shunts between base metallization and emitter doping [225, 229]. Burried emitter structure allows for using similar area fractions for base and emitter metallization, without the need for any dielectric insulation. Reprinted with permission from [225], N.-P. Harder, V. Mertens, and R. Brendel, Buried emitter solar cell structures: Decoupling of metallisation geometry and carrier collection geometry of back contacted solar cells, phys. stat. sol (RRL), 2 (2008) 148. Copyright © 2008 published by John Wiley & Sons. Permission granted. License number 3582490855869

3.5 Current developments for the low-cost IBC solar cell processing

Currently the focus in the processing of the IBC cells is on simplifications of the process flow, and overall cost reduction. The examples below show selected approaches to reduce the processing complexity, and cost of the IBC cells.

3.5.1 Ion-implantation

Due to its directional character, the ion-implantation process allows for one-step patterning of the doped regions. This means that in the ion-implantation process only one
single surface of the wafer is modified. Thus, unlike in the high-temperature diffusion process, there is no need to carefully protect the other (non-modified) surface during the implantation step. This feature of ion implantation can potentially allow for major simplifications in the processing of the complex rear side structure of the IBC cells. Moreover, a single high-temperature annealing process, at the final stage of the IBC cell processing, can deliver growth of the front and rear side Si oxide passivation layer and anneal multiple doping processes. A possible process flow to manufacture high-efficiency IBC cells with ion implantation is shown in Fig. 23. An ion-implantation application to the production of high-efficiency IBC cells is under development by various industrial and research groups [140, 230, 231]. In this example the front side oxide is removed (process step: oxide etch front) in order to grow a thin passivation oxide on the front surface, for the subsequent ARC SiN.

Fig. 23 Example of a process flow used for processing of ion implanted IBC cells [230]. Ion implantation process allows one-step patterning of doped areas. Processing steps can be simplified by using ion implantation process. Multiple dopants can be annealed in a single annealing process. With permission from [230], N. Bateman, P. Sullivan, C. Reichel, J. Benick, M. Hermle, “High quality ion implanted boron emitters in an interdigitated back contact solar cell with 20% efficiency”, Energy Procedia 8 (2011) 509. Copyright © 2011 Published by Elsevier Ltd. Permission granted. License number 3584831043918.

3.5.2 IBC c-Si back heterojunction solar cells

Heterojunctions are known for their excellent surface passivation properties. Their application to the IBC solar cells can therefore improve the open circuit voltages significantly. At the same time, the deposition of the a-Si:H layers can be done through a mask at low-temperatures, which offers a potential of reduction of the complexity of the IBC cell process flow [232-234]. Si based back heterojunction solar cells are presented in Sec.5.
3.5.3 Epitaxial doping layers

Another opportunity for the simplification of the processing flow for the IBC cells is the epitaxy for the formation of the highly doped regions. Epitaxy is the method of deposition of the respective material on a crystalline wafer, in which the deposited material maintains the crystallographic orientation of the crystalline wafer. The technological process of epitaxy allows for the precise formation of the doping profiles, which are not possible to achieve with the traditional high-temperature diffusion process. A study by Baker-Finch and Basore [235] demonstrated the potential of the epitaxy process in the formation of the front surface field layer in the IBC cells.

3.5.4 Laser processing and screen-printing for low-cost structuring of IBC cells

The masking steps to process IBC cells are often performed using photolithography, which is costly and thus not applicable for mass production of IBC cells. Low-cost and high-throughput alternatives to photolithography are being developed and applied in the processing of IBC cells. These structuring alternatives include laser processing and screen-printing processes. Engelhart et al. demonstrated IBC cells with efficiency of 22% with application of laser structuring [196]. Granek et al. applied screen-printed processes for masking of the IBC cells to reach 21.3% efficiency [217]. Examples of the low-cost IBC cell processes with the focus on applying the screen-printed metallization on IBC cells were developed by Halm et al. [236], Castano et al. [237], Galbiati et al. [238], and Lamers et al. [239]. Wohl et al. [240, 241] developed an industrially feasible IBC process with the Al alloyed emitter, to eliminate the boron diffusion process. This process flow is shown in Fig. 24.
Fig. 24 Process sequence for all-screen-printed IBC cell with Al alloyed emitter on an n-type wafer [240].

3.5.5 Formation of the interdigitated metallization grid

The formation of the interdigitated metallization grid is often achieved using photolithography masking and thermal evaporation of the metal layers. However, as
mentioned earlier, photolithography is not cost-effective for solar cell production. Different methods to create interdigitated metallization grid from the full area deposited (e.g. by the means of thermal evaporation or sputtering) metal layer are under evaluation. These include: (i) bi-level metallization scheme proposed by Sinton et al. [242] and currently under development by De Vecchia et al. [243], (ii) self-aligned metallization scheme proposed by Sinton in 1988 [186], (iii) laser ablation of the masking layer and etching of the bulk metal [244], (iv) local etching of the metal layers through screen-printed masks [184], and (v) lift-off and laser assisted lift-off using screen-printed layers [184]. There exist another approach to metallization, namely direct plating of metal on the rear cell surface, which has been investigated for the front side metallization of the standard c-Si solar cells [245].

Broadly, research advances in this field have not been reported widely so far, which indicated a potential for further cost reduction and process flow simplifications in the processing of c-Si IBC solar cells.

3.6 Future outlook

Recetly Panasonic and Sharp [246,247] research laboratories have reported efficiencies of over 25 % at the laboratory scale for IBC solar cells, and the milestone of 26 % efficiency seems to be practically achievable with the single-junction c-Si IBC cell. These groups combine an IBC cell structure with high level of surface passivation for the metal contact regions using a heterojunction of a-Si:H/c-Si interfaces. Currently recombination losses at the metallized areas are one of the dominant recombination mechanisms in high-efficiency IBC cells. Therefore research efforts are currently focused on the introduction of industrially feasible passivated contact concepts with the goal of drastically reducing minority-carrier recombination rate at the metal contacts. One important area of recombination is at the edge. It is expected that in the future the best efficiencies of IBC cells would be reported on large solar cell surfaces, where the relative impact of the edges will be
low. The next significant modification to the IBC cell structure may be the application of a novel module interconnection technology based on patterned back-sheet foil [181]. Such interconnection will allow for eliminating the necessity of complicated metallization busbar and finger grids on the IBC cells side, and will allow for more design freedom for the solar cell engineers. This can potentially have a positive impact on the efficiency and packaging density of the solar cells in a module.

4. Crystalline Si based solar cells: Front heterojunction

A-Si:H/c-Si front heterojunction (hereafter called Si heterojunction or SHJ) solar cells are fabricated by deposition of a few nm thin intrinsic a-Si:H followed by doped a-Si:H onto (typically) c-Si wafers. Their working principle is very similar to conventional Si wafer cells with diffused junctions; it can be summarized briefly as follows (Fig. 25): The incident light generates electron-hole (e-h) pairs in the c-Si wafer. The minority charge carriers are collected on the cell’s front side by the Si heterojunction, and are laterally transported towards the metal front grid through a thin transparent conducting oxide (TCO) layer that also acts as an anti-reflection coating. Majority charge carriers are collected by the BSF, which is also formed by an a-Si:H/c-Si heterojunction. The rear side contact is completed by a full area metallization. Often, another TCO layer is inserted between the a-Si:H and metal on the back side to improve the optical properties of the cell in the infrared part of the spectrum.

4.1 Introduction

Si heterojunction device architecture enables very high energy conversion efficiencies of 24.7% on industrially relevant cell sizes (>100cm²) [248] and above 21% (>18% module efficiency) in industrial production [249]. The key feature of this technology is that the metal contacts, where the recombination velocity is high in traditional diffused-junction cells, are
spatially and electronically separated from the absorber by insertion of a wider bandgap a-Si:H layer. This general idea was introduced by Fuhs et al. in the 1970s using a direct heterojunction between doped a-Si:H and c-Si [250] and augmented by the company Sanyo in the 1990s with the introduction of a low-defect intrinsic a-Si:H buffer layer between the doped a-Si:H and the c-Si wafer [251]. It enables $V_{oc}$s above 700 mV. Furthermore, the cell process is based on comparatively simple full-area deposition steps and screen-printed contacts, whereas in conventional c-Si cells with diffused emitters, efficiencies well above 20% can only be reached using local contacting schemes, which require expensive patterning techniques. Additionally, since all process steps occur at temperatures around or below 200°C, the cell has a low thermal budget [252]. In contrast to conventional diffusion processes that lead to wafer bowing and increased breakage, the SHJ process is compatible with very thin wafers (the 24.7% cell was fabricated on a 98 µm thin wafer) or Si absorbers on glass with a thickness of few µm, which have indeed lately shown promising $V_{oc}$s and efficiencies of up to 656mV and 11.8%, respectively [253, 254].

Many aspects of the SHJ device concept will be discussed only briefly in the following. For further reading, an extensive review article on SHJ solar cells published by de Wolf et al. [255], and a monograph [256] on the same subject are recommended.
4.2 c-Si based front heterojunction cell design – an overview

Figure 25 Schematic cross-section and energy band diagram of a p-type a-Si:H/intrinsic a-Si:H/n-type c-Si heterojunction solar cell. The intrinsic a-Si:H acts as passivation layer between c-Si (absorber) and recombination active metal (or TCO) contacts. Both p-n junction and BSF are formed by a-Si:H/c-Si heterojunctions. $E_c$, $E_v$ are the band edges, $\Delta E_c$, $\Delta E_v$ the band offsets between the intrinsic a-Si:H and the c-Si, $E_F$ the Fermi level and $D_T$ the density of defect states at the intrinsic a-Si:H/c-Si interface. Note the asymmetry of the band offset: $\Delta E_v$ is much larger than $\Delta E_c$. For clarity, texturization of the wafer is not shown.

In SHJ cells, a-Si:H/c-Si heterojunctions are used to form the p-n junction and BSF of the cell. Figure 25 shows a simplified sketch of this cell type, including the intrinsic buffer layers, together with a schematic band diagram. Note that the usual texturization of the wafer has been omitted for clarity. As already mentioned above, the Si heterojunction is the solution to the conflicting requirements to (i) passivate electronically the surfaces of the c-Si absorber, where charge carriers are photogenerated, in order to obtain a large splitting of the quasi Fermi levels and thereby a high $V_{oc}$, and to (ii) extract the photogenerated charge carriers efficiently through the same surfaces, yielding a low series resistance/high fill-factor. In the SHJ concept, this problem is solved by inserting a passivating, semiconducting film between the absorber and the highly recombination active metal (or TCO, see below) contacts. This passivating a-Si:H film, in turn, is usually divided into two parts, i.e. the passivation layer proper, consisting of low-defect not intentionally doped (intrinsic) a-Si:H and a doped, more defective a-Si:H layer that induces the appropriate band bending to form the p-n junction or
the BSF. Electrical contacts to the cell are then formed using TCOs and a metallization layer (grid/full-area).

The main differences between semiconductors in the Si heterojunction cell and the equivalent homojunction cell are:

(i) **Abrupt interfaces:** In contrast to the usual diffused emitter and BSFs, the Si heterojunction is abrupt on the monolayer length scale. Thus the doping profile usually is a step function. Similarly, it is believed that the second heterojunction in the cell, the TCO/n-a-Si:H junction, should also be as abrupt as possible.

(ii) **Defect states in the a-Si:H bandgap and at the a-Si:H/c-Si interface:** These are an intrinsic property of overconstrained semiconducting glasses in general [257]. They consist of the so-called Urbach tails, i.e. exponential distributions of electronic states reaching from the band edges into the bandgap of the material, and of unsaturated, dangling Si bonds deep in the bandgap, which can be saturated by the hydrogen present in the a-Si:H film. At the a-Si:H/c-Si interface, surface contamination by atoms or molecules adsorbed to the c-Si wafer surface prior to a-Si:H deposition can lead to additional extrinsic defect states at the interface. Controlling surface contamination and the initial stages of a-Si:H growth are therefore key issues to obtaining low defect density a-Si:H/c-Si interfaces.

(iii) **Band offsets:** The difference in $E_g$ between c-Si ($E_g \sim 1.12$ eV at room temperature) and a-Si:H ($E_g = 1.6$-1.9 eV, depending on deposition conditions) gives rise to discontinuities in the valence and conduction band edges, usually denoted by $\Delta E_V$ and $\Delta E_C$, respectively, see the schematic band diagram in Fig. 25. Band offsets also exist at the TCO/a-Si:H interface.

For the contact layers, the differences to conventional homojunction cells are:

(iv) **TCO:** Instead of the usual SiN ARC, SHJ cells use TCO, which provide both the ARC properties as well as a high lateral conductivity. This is necessary because even the conductivity of doped a-Si:H films is smaller by orders of magnitude. Thus, charge transport
proceeds essentially perpendicular through the entire a-Si:H/c-Si/a-Si:H cell structure (Fig. 25), then laterally through the TCO to the contact fingers.

(v) **Metallization:** For industrially relevant cell processes, screen printing is widely used. Pastes for SHJ cells must yield good electrical properties for curing temperatures around 200°C, which necessitates the use of a relatively high content of Ag. Lately, electroplated contacts have also been introduced successfully [258,259].

Conceptually, the SHJ band offsets (i.e., band-edge misalignments) are the main difference to the p-n homojunction. They are an experimental approximation of the idea that contacts to a solar cell should act as a semi-permeable membrane through which charge carriers are extracted [260]. The unwanted charge carriers in the vicinity of a contact – i.e. the minority-carriers at the BSF, and the majority carriers at the p-n junction – are hindered by the band offsets in the heterojunctions and the low conductivity of the doped a-Si:H for the unwanted carrier polarity to reach the cell contacts, and thereby recombination at the contacts is effectively suppressed. Thus, a high separation of quasi-Fermi levels is obtained, and low reverse diode saturation currents and high \( V_{oc} \) can be expected in the cell. The advantage of having suitable band offsets at the contacts of a solar cell, similar to the case of heterostructure lasers, has been pointed out already in the 1980s, and their benefit to cell \( V_{oc} \) has been shown for the SiO\(_x\)/c-Si tunnel-heterojunction case, in the so-called semi-insulating polysilicon cell [261]. Another similar device is the metal-insulator-semiconductor cell [262], where a thin oxide layer acts as the semi-permeable membrane that has to be traversed, in this case by tunneling.

### 4.3 c-Si wafers, surface texture and cleaning

SHJ cells can be realized on both n- and p-type wafers, although the highest cell efficiencies have been demonstrated on n-type [263]. Typical doping levels are in the range also used for homojunction cells, 1-5 \( \Omega \)-cm. In order to realize the high \( V_{oc} \) potential of SHJs,
a high minority charge carrier lifetime, i.e. low density of recombination-active defects in the
design is needed. A bulk minority-carrier lifetime of several milliseconds for generation rates
corresponding to air mass 1.5 (AM1.5) illumination is desired. Today, with improved crystal
growth technology, this carrier lifetime range is readily achievable in low-cost Cz wafers.

As explained in Sec.2, the wafers are textured to improve light trapping, usually with
a random pyramid texture, and thoroughly cleaned using the so-called RCA process
developed as a standard cleaning process by the Radio Corporation of America [41] or a
variant thereof. The native Si oxide layer grown in the last process is then usually removed
by a short etch in diluted HF (1%, 1 min) immediately before the wafer is loaded into the
PECVD system for a-Si:H deposition. Alternative pre-cleaning and oxide removal steps
(chemical smoothing of wafer surface) have also been explored [264].

Fig. 26 SEM images of textured Si wafers: (a) after 5μm side damage etch removal and 20min texture etching
time; (b) after 10μm side damage etch removal and 10min texture etching time. Scanning size of both images:
25μm × 19μm, tilt: 30°; (c and d) histograms of the statistical analysis of the corresponding pyramid sizes in the
SEM images above. Data is obtained from at least 3 measurements at different positions on the sample.
Reprinted with permission from [265], Bert Stegemann, Jan Kegel, Mathias Mews, Erhard Conrad, Lars Korte,
Uta Stürzebecher, Heike Angermann "Passivation of Textured Si Wafers:Influence of Pyramid Size
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Recently, the influence of the random pyramid surface topology has been investigated
in detail. Figure 26 shows that the morphology can be modified within a wide range to yield
either mostly smaller pyramids or a broader distribution with predominantly large or very large ones. When passivated with a-Si:H, these surfaces behave very differently (Fig. 27). The effective minority charge carrier lifetime, a measure for the $V_{oc}$ potential in cells produced with such passivation layers, increases strongly when the fraction of small pyramids is reduced [265]. It can be surmised that this behavior is related to the difficulty of growing well-passivating layers in the valleys and at edges of the pyramids [266]. With decreasing fraction of small pyramids, the line density of such valleys and ridges also decreases.

Fig. 27 Dependence of the effective carrier lifetime on the fraction of small pyramids. As can be seen, carrier lifetime increases when the fraction of small pyramids is reduced. This is probably due to the poor passivation quality in the valleys and edges of the pyramids. Reprinted with permission from [265], Bert Stegemann, Jan Kegel, Mathias Mews, Erhard Conrad, Lars Korte, Uta Stürzebecher, Heike Angermann "Passivation of Textured Si Wafers: Influence of Pyramid Size Distribution, a-Si:H Deposition Temperature, and Post-treatment." Energy Procedia, 38(2013)881. Copyright © 2013 The Authors. Published by Elsevier Ltd. License number 3472391033286.

4.4 Hydrogenated amorphous Si

As sketched in Fig.25, the emitter and BSF contacts of SHJ solar cells consist of doped and intrinsic a-Si:H films with a thickness of the order of 10 nm. These films are grown using PECVD at deposition temperatures around 200°C, with growth rates of the order of 10 nm per minute. Precursor gases for undoped a-Si:H films are SiH₄ and hydrogen (H₂).
Doping is usually achieved by admixture of phosphine (PH₃) for n-type and diborane (B₂H₆) or trimethylboron (B(CH₃)₃) for p-type doping. Generally, processes are similar to those used for a-Si:H thin-film p-i-n solar cells. In the field of SHJ cells, most results have been reported for a-Si:H grown in conventional parallel plate reactors with radio frequency (RF, 13.56 MHz) excitation, [267-269]. However, it appears that suitable deposition regimes can be found for most PECVD and related a-Si:H deposition techniques. Good surface passivation properties and/or solar cells have also been reported for a-Si:H grown with very high frequency (VHF ≥ 40 MHz) excitation [263], hot-wire chemical vapor deposition (CVD) [270], DC saddle field PECVD [271], electron cyclotron resonance (ECR)-CVD [272] etc.

The insertion of thin (2-8 nm) intrinsic a-Si:H interlayers for c-Si surface passivation between the c-Si wafer and the doped a-Si:H films used to form the p-n junction or BSF can be seen as a breakthrough for realizing the unique potential of SHJ cells, namely their outstandingly high Voc. Indeed, Sanyo had patented this use of an intrinsic a-Si:H buffer and named their solar cells accordingly as heterojunction with intrinsic thin layer (HIT) cells [251]; the patent for the intrinsic buffer layer expired in 2011. This prompted attempts to achieve good cell performance also without using intrinsic a-Si:H (i-a-Si:H) layer with, at the time, notable results of 19.8% and 18.4% efficient cells for p-type a-Si:H/n-type c-Si and the inverse cell structure, respectively [273, 274]. However, Voc's were generally much lower, of the order of only 630-640 mV. This is related to a doping-dependent defect generation mechanism in a-Si:H, as discussed below in Sec. 4.4.2. Thus, it is indeed essential to passivate the c-Si surface to reduce the density of defect states (Dit) in the bandgap (Fig. 25) by saturating dangling bonds at the c-Si surface using a low-defect i-a-Si:H layer.
4.4.1 Intrinsic a-Si:H films

Many studies conducted in the past years have led to the conclusion that the microscopic structural and electronic configuration of ultrathin a-Si:H layers is governed by the same mechanisms as that of thick a-Si:H films, as described, for example, in Ref. [275,276]. The deposition conditions systematically affect the layer properties, and a combination of low-temperature deposition and a subsequent anneal was shown to yield best results in terms of a-Si:H/c-Si interface passivation. Interestingly, not only conventional hot plate anneals for several minutes, but also accelerated annealing using microwave radiation can be used. The latter process requires only a few seconds [277]. Furthermore, a cyclic sequence of short a-Si:H deposition and hydrogen plasma steps [278] or a post-treatment of the grown layer with a hydrogen plasma [279] have been useful in improving a-Si:H/c-Si interface passivation.

Fig. 28 Schematic sketch of the density of states (DOS) in the valence and conduction band of a-Si:H on the (a) linear and (b) semilog scale. The states occupied by electrons are marked as hatched area (left side), after [276]. Urbach tails (i.e. exponential distribution of electronic states from band edges into the bandgap) are induced by strain in the amorphous network. Occupied DOS as measured by using near-ultraviolet photoelectron spectroscopy, linear and semilog scale (right side). Reproduced with permission from [256], Wilfried G. J. H. M. van Sark, Lars Korte, Francesco Roca, Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells, 2011. Springer, 2011. Copyright © Springer-Verlag Berlin Heidelberg. License number 3498221350973.

The density of states of a-Si:H is depicted in Fig. 28. In the valence and conduction bands, it is similar to that of c-Si, but has additional defect states in the bandgap. Urbach tails
decay exponentially into the bandgap and are induced by strain in the amorphous network, whereas a broad distribution of defects near midgap consists of dangling (broken/unsaturated) Si-Si bonds, with density \( N_d \). The exponential slope of the Urbach tails, the so-called Urbach energy \( (E_0) \), is a measure for the overall strain in the amorphous network (increased \( E_0 \) means increased strain), and dangling bonds are created when the strain in the bonds forming the Urbach tails becomes too large. Thus, it is intuitively clear that \( E_0 \) and the dangling bond density are related. Broadly speaking, if the a-Si:H network is in thermodynamic equilibrium, an increase in \( E_0 \) also yields an increased \( N_d \). This is the gist of defect generation models proposed by Stutzmann [280] and by Powell & Deane [281,282]. The latter, so-called defect pool model also considers electronic contributions to the system’s free energy, which makes \( N_d \) and its distribution across the bandgap dependent on the position of the Fermi level.

Electronically, the a-Si:H bandgap defects behave differently. While the band tail states act as traps for charge carriers from the band they are originating from, dangling bonds deeper in the gap are recombination centers. Dangling bonds are amphoteric defects, i.e., the \( sp^3 \) hybridized orbital of the dangling bond can be occupied by 0, 1 or 2 electrons, leading to the charge states \( D^+ \), \( D^0 \) and \( D^- \). In the single-electron band diagram picture, the energy positions for the possible transitions of the dangling bond from unoccupied to singly occupied, \( D^{+0} \), and from singly to doubly occupied, \( D^{0-} \), are represented by two Gaussian distributions in the bandgap [281-283]. The \( D^{+0} \) states have donor character, the \( D^{0-} \) states are acceptor-like. In the description of recombination, this amphoteric character of the defects leads to a behavior that differs from the conventional Shockley-Read-Hall formalism [283-285].
Fig. 29 Valence band offsets of i-a-Si:H/n-c-Si heterostructures with varying hydrogen content. The conduction band offset is determined based on the valence band offset, using the optical bandgap of the a-Si:H films as determined from spectral ellipsometry. As hydrogen content increases in the film, the main variation occurs in $\Delta E_V$ while $\Delta E_C$ is almost constant. For state of the art a-Si:H films (with 10-15% hydrogen) $\Delta E_V$ and $\Delta E_C$ are approximately 0.45 eV and 0.25 eV, respectively. Reproduced from [286] with permission, T. F. Schulze, L. Korte, F. Ruske, and B. Rech, Band lineup in amorphous/crystalline silicon heterojunctions and the impact of hydrogen microstructure and topological disorder, Phys. Rev. B 83 (2011) 165314. Copyright © 2011 American Physical Society. License number 3583611410416.

The deposition of a-Si:H on a c-Si wafer leads to the formation of a type I heterojunction (straddling gap, i.e., the gap of the smaller bandgap material is completely within the gap of the wider bandgap material). Thus, as can be seen from Fig. 25, the band offset at the a-Si:H/c-Si interface acts as barrier for both electrons and holes coming from the c-Si wafer. The value of the valence band offset $\Delta E_V$ can be determined reliably using near-UV photoelectron spectroscopy [287-289]. As the bandgap of a-Si:H can be varied by changing the hydrogen content of the film, the band offsets also have to vary. As shown in Fig. 29, it was found that the main variation occurs in $\Delta E_V$, whereas $\Delta E_C$ is almost unchanged [286]. State of the art a-Si:H films (hydrogen concentration 10-15%) have $\Delta E_V \sim 0.45$ eV, $\Delta E_C \sim 0.25$ eV. No variation of the bandgap with film thickness or doping was found [288]. To date, there exist no systematic investigations of the influence of the increase in $\Delta E_V$, i.e., in the barrier for hole transport, on solar cell properties.

At the a-Si:H/c-Si interface (Fig.25), as-deposited $D_{th}/cm^2$ is determined by the local network structure at the interface, which is in a non-equilibrium state for samples deposited at
low-temperature [267]. The subsequent annealing step leads to thermodynamic equilibration
between the a-Si:H bulk and the a-Si:H/c-Si interface. The equilibrated a-Si:H/c-Si interface
region then does not possess unique electronic properties but is determined by the a-Si:H bulk
density of states distribution [290]. The a-Si:H bulk volume defect density \( (N_d) / \text{cm}^3 \) is
related to the a-Si:H/c-Si interface defect density by the relation
\[ D_{it} = N_d \times d_i, \]
d\( d_i \) is the
characteristic length, in the nm range, over which charge carriers generated in the c-Si wafer
can travel into the a-Si:H and then recombine via a-Si:H defects. A calculation based on the
assumption that the charge carriers tunnel into the a-Si:H yields \( d_i = 2.7 \text{ nm} \) [291]. Indeed,
recombination at the a-Si:H/c-Si interface can be described consistently using a projected a-
Si:H density of states as c-Si surface defect density of states [284].

For high \( J_{sc} \), photogeneration in the c-Si absorber must be maximized. Thus, it is
desired to reduce parasitic absorption in the a-Si:H layers by reducing their thickness. Fig. 30
shows an example of typical findings. Here, the \( J_{sc} \) decreases with a slope of \( \sim 0.1 \text{mA/cm}^2 \) per
additional nm of i-a-Si:H buffer layer thickness. However, it is found that a minimum i-a-
Si:H buffer layer thickness of 5nm or slightly below is needed. For even thinner films (<5
nm), the a-Si:H/c-Si interface passivation breaks down, therefore \( V_{oc} \) is reduced and the cell’s
fill factor also decreases [292].
Fig. 30 Output characteristics of 4cm² solar cells with varying i-a-Si:H layer thickness. Each data point represents the average value of three cells, except the data for the thickest layer, for which only one cell was measured. The gray triangles in (a) represent the implied $V_{oc}$ of the cells prior to ITO deposition and metallization, determined from quasi-steady-state photoconductance (Sinton) measurements. The dashed line in (b) is the calculated dependence of $J_{sc}$ on i-a-Si:H layer thickness. Reproduced from [292] with permission, Holman, Z.C.; Descoeudres, A.; Barraud, L.; Fernandez, F.Z.; Seif, J.P.; De Wolf, S.; Ballif, C., Current Losses at the Front of Silicon Heterojunction Solar Cells, IEEE Journal of Photovoltaics, 2 (2012)7. Copyright © 2012, IEEE. License number 3498231121849.

4.4.2 Doping of a-Si:H - formation of the p-n junction and doping induced defects

The a-Si:H film stack for the p-n junction and the BSF is completed by the deposition of doped a-Si:H layers on the i-a-Si:H buffers. As shown in Fig. 31, for increasing n-type doping of ~10 nm thin a-Si:H films, the defect density in a-Si:H increases with doping level, a behavior already well known for thick a-Si:H films [275]. Therefore, an optimum a-Si:H doping level exists for SHJ cells. For high doping levels, the increase in band bending at the heterojunction, which is beneficial for forming a well-working p-n junction (high cell $V_{oc}$ and efficient carrier extraction, thus high fill factor, at the maximum power point), is balanced against increasing defect concentration. The latter is detrimental due to the enhanced recombination rate at the interface and in the a-Si:H layers. This is exemplified in Fig. 32 for n-a-Si:H/p-c-Si solar cells without i-a-Si:H buffer: While the built-in potential of the p-n junction $\Phi_0$ increases up to a gas phase doping of $10^4$ ppm, $V_{oc}$ reaches a (rather low, due to the missing i-a-Si:H) maximum already at a moderate doping of ~2000 ppm and is reduced for higher doping. The minority-carrier lifetime $\tau_{ini}$ (in this case measured by surface photovoltage) follows the same trend as the $V_{oc}$: As shown in Fig. 32, lower panel, $\tau_{ini}$ peaks at the same doping level as the $V_{oc}$. Clearly, at doping levels above 2000 ppm, the increasing defect density at the a-Si:H/c-Si interface overcompensates the still (up to $10^4$ ppm) slightly improving field effect passivation.
Fig. 31 Density of occupied states in the a-Si:H bandgap for increasing gas phase doping \( ([\text{PH}_3]/[\text{SiH}_4] = 0 \ldots 10,000 \text{ ppm}) \), arrows mark the Fermi level position (left side). Defect parameters, viz. valence band Urbach energy, energetic position and density of the dangling bond defect distribution (right side). As can be seen (right side), by increasing n-type doping in the a-Si:H film, defect density increases with doping level. Reproduced from [293], with permission, L. Korte, and M. Schmidt, Investigation of gap states in phosphorous-doped ultra-thin a-Si:H by near-UV photoelectron spectroscopy, J. Non-Cryst. Sol. 354 (2008) 2138. Copyright © 2008 Elsevier B.V. License number 3472101463232.

Fig. 32 Upper panel: built-in potential \( \phi_0 \) (circles) and solar cell \( V_{oc} \) (lozenges, rescaled to eV units). Lower panel: surface photovoltage decay time constant \( \tau_{ini} \). A heterojunction was formed between n-a-Si:H and p-c-Si without using a buffer layer (intrinsic a-Si:H). Note that minority-carrier lifetime \( (\tau_{ini}) \) and \( V_{oc} \) peak at the same doping level. \( V_{oc} \) reaches a maximum at a doping level of 2000ppm and then decreases for higher doping. The built-in-potential increases up to a doping level of \( 10^4 \text{ ppm} \), then decreases slightly for higher doping. Reproduced with permission from [256], Wilfried G. J. H. M. van Sark, Lars Korte, Francesco Roca, Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells, 2011. Springer, 2011. Copyright © Springer-Verlag Berlin Heidelberg. License number 3498221350973.

For doped a-Si:H deposited on i-a-Si:H buffer layers, an additional effect has to be considered: As shown by de Wolf et al. the shift in the i-a-Si:H Fermi level induced by deposition of the doped a-Si:H film on top of the i-a-Si:H leads to Si-Si bond rupture in the i-
a-Si:H buffer layer, i.e. generation of additional defects in the i-a-Si:H that counteract the movement of Fermi energy ($E_F$) and are recombination-active [294]. It can be surmised that this effect is closely related to the defect equilibration mechanisms described by the Fermi-level dependence of defect creation in the defect pool model.

4.5 TCOs for SHJ heterojunction cells

The TCO’s role in SHJ cells is two-fold: (i) to provide sufficiently low contact and sheet resistance in order to transport the charge carriers coming from the a-Si:H to the metal contacts, and (ii) to act as an ARC, i.e. to maximize light incoupling into the solar cell. The quasi-standard TCO material in SHJ cells is ITO, another option is Al-doped zinc oxide (ZnO:Al) as shown in Fig.33, more recently indium oxide (In$_2$O$_3$) doped with hydrogen (In$_2$O$_3$:H) [295] or hydrogenated tungsten-doped In$_2$O$_3$ [296] have also been used.

TCOs are degenerately doped wide bandgap semiconductors ($E_g$ typically >3 eV): To fulfill the requirement (i), $R_{sh} < 100 \, \Omega/$sq is desired. Furthermore, the required refractive index around 2 together with the necessity to achieve destructive interference in the 600 nm range lead to a thickness of the order of $d_{TCO} = 80$ nm. Maximum carrier mobility ($\mu$) is in the order of 10 to 70 cm$^2$/Vs, thus with $R_{sh} = 1/(q \, N \, \mu \, d_{TCO})$, carrier concentrations ($N$) in the range of $10^{20}$/cm$^3$ are required. Such high carrier concentrations lead to a widening of the optical bandgap (Burstein-Moss shift), partially offset by a bandgap narrowing due to electron-impurity many body interactions, and an appreciable free carrier absorption in the longer wavelength range around the c-Si bandgap wavelength [292,297, 298]. Figure 33 shows an exemplary comparison of simulated 1 – R and external quantum efficiency (EQE) curves for a HIT solar cell on flat wafer for various doping levels of a 85nm thick front ZnO:Al layer [299]. It is apparent from the simulation that for higher TCO doping, current is lost in the device due to inferior anti-reflection properties of the highly doped films (1 – R decreases) and increasing absorption in the TCO (area between 1 – R and the EQE increases).
Comparison between the simulation (Fig. 33, left side) and experimental data obtained from ZnO:Al and ITO used as TCOs in HIT cells (Fig. 33, right side), shows that ZnO:Al yields a higher EQE due to the lower carrier concentration in the ZnO:Al. Further details can be found elsewhere [299].

![Comparison between the simulation (Fig. 33, left side) and experimental data obtained from ZnO:Al and ITO used as TCOs in HIT cells (Fig. 33, right side), shows that ZnO:Al yields a higher EQE due to the lower carrier concentration in the ZnO:Al. Further details can be found elsewhere [299].](image)

Another aspect that has to be considered in optimizing a TCO for the use in SHJ cells is the band alignment with the a-Si:H (Fig. 25). As shown in Fig. 34, the work function of the TCO plays an important role for the solar cell parameters. In the simulated case, a work function difference of only 0.1 eV between the TCO and the p-a-Si:H emitter already leads to an appreciable decrease in $V_{oc}$ and, more pronouncedly, fill factor [299]. The reason is that on top of the desired p-n junction diode, an undesired counter diode is formed by the TCO/doped a-Si:H junction. This is depicted schematically in Fig. 35, where an equivalent circuit consisting of the p-n diode and the TCO/p-a-Si:H counter diode with a parallel shunt resistance is sketched. These two diodes together with the resistance indeed yield a calculated current-voltage (I-V) curve that can go from slightly decreased fill factors to S-shapes. Such
S-shaped I-V curves are observed experimentally [300,301] and also in numerical simulations such as the one used to generate Fig. 34 [302].

Fig. 34 Simulated solar cell parameters as a function of the work function difference between the TCO and the p-a-Si:H layer for different distances of the Fermi-level from the valence band. Between TCO and p-a-Si:H emitter, even a work function difference of 0.1eV leads to a significant decrease in $V_{oc}$ and fill factor. This is due to an undesired counter diode formed by the TCO/doped a-Si:H junction. Reprinted with permission from [299], R. Rößler, C. Leendertz, L. Korte, N. Mingirulli, and B. Rech, Impact of the transparent conductive oxide work function on injection-dependent a-Si:H/c-Si band bending and solar cell parameters, Journal of Applied Physics 113 (2013) 144513. Copyright © 2013 American Institute of Physics. License number 3472401268226.

Fig. 35 Sketch of the TCO/a-Si:H/c-Si interface region, together with an equivalent circuit consisting of the desired a-Si:H/c-Si p-n junction and an antiparallel, parasitic TCO/a-Si:H diode (left side). Resulting I-V curve and contributions of the two diodes (right side). A parasitic diode is formed when there is a work function difference between TCO and doped a-Si:H. After [303], with permission, R. Rößler, L. Korte, C. Leendertz, N. Mingirulli, M. El Mhamdi, and B. Rech, ZnO:Al/(p)a-Si:H Contact Formation and Its Influence on Charge Carrier Lifetime Measurements, edited by G. Willeke, H. Ossenbrink, & P. Helm. Proc. 27th European Photovoltaic Solar Energy Conference and Exhibition, Munich: WIP Munich, 2012, p.1443.

This problem of an unsuitable work function is a general one for the usual n-type TCOs forming junctions with p-a-Si:H. However, it appears that it is less pronounced for the case of
ITO than for ZnO:Al [299,303]. Still, one might speculate that this is a possible reason for the consistently lower fill factors in SHJ cells as compared to diffused junction cells with similar $V_{oc}$ [255,290].

4.6 Charge transport in SHJ: I-V curves and device operation

For the SHJ cell, charge transport across the junctions may proceed both by diffusive transport as well as by tunneling processes, the detailed transport mechanisms being dependent on the materials properties (defect densities, bandgap/band offset height) as already discussed above, and also on the regime of the applied bias voltage. Under high forward bias, at the operating point of the cell, diffusive transport prevails at least in state-of-the art SHJ cells, and indications for tunnel transport are found in low forward and reverse bias [268,304,305]. If, for example, the band offset for the holes at the p-a-Si:H/n-c-Si contact depicted in the band diagram of Fig.25 becomes too high, charge carrier transport can be hindered because the charge carrier has to overcome the band offset barrier by thermionic emission or tunneling processes. Depending on the details of charge distribution and recombination at the heterointerface, this can manifest in the solar cell characteristics curve as an effect similar to a series resistance, or in an S-shaped I-V curve, [300,306] which, however, can also arise from the TCO/a-Si:H junction, as mentioned above. On the other hand, an increased band offset can also decrease the cell’s sensitivity to high defect densities at the a-Si:H/c-Si junction. This is depicted in the simulation result in Fig.36, where together with a general trend of increasing cell efficiency with increasing minority-carrier band offset (in this case, $\Delta E_C$, because an n-a-Si:H/p-c-Si cell is simulated), it is also observed that the drop in cell efficiency for increasing a-Si:H/c-Si interface defect densities is less severe if $\Delta E_C$ is large.
Fig. 36 Dependence of the simulated efficiency of n-a-Si:H/p-c-Si solar cells on the minority-carrier band offset and the interface trap density ($D_{it}$) at the a-Si:H/c-Si interface. Cell efficiency increases with increasing minority-carrier band offset ($\Delta E_c$). An increased band offset decreases the cell’s sensitivity to high defect densities at the n-a-Si:H/p-c-Si junction. Also, the drop in cell efficiency is less severe (for increasing $D_{it}$ at the a-Si:H/c-Si interface) when $\Delta E_c$ is large. After [300], Froitzheim, A., K. Brendel, L. Elstner, W. Fuhs, K. Kliefoth, and M. Schmidt. "Interface recombination in heterojunctions of amorphous and crystalline silicon." J. Non-Cryst. Sol. 299-302 (2002) 663.

State of the art SHJ cells can be described very well with the usual 2-diode-model plus series and parallel resistance. Furthermore, it was found that the description of an a-Si:H/c-Si cell in high forward bias, i.e. notably, at the maximum power point, or $V_{oc}$, can be carried out in terms of the simple Shockley diffusion model, just as for (ideal) homojunction solar cells [268]. The SHJ cell essentially behaves like a single-sided junction (space-charge region only in the c-Si, recombination at the a-Si:H/c-Si interface), with one important difference:

The analysis of the ideality factor ($n_1$) and activation energy of the reverse saturation current carried out in [268] shows that the heterojunction aspects of carrier transport across the p-n junction become more pronounced with enhanced interface passivation, and are responsible for a deviation from the ideal value of $n_1 = 1$.

### 4.7 Double sided SHJ solar cells - state of the art

De Wolf’s review [255] provides an excellent and comprehensive overview on the R&D groups working on SHJ cells and their best published results. In the following, some important results are mentioned and updates are given. Note that single-sided SHJ cells are excluded from this summary, since they are discussed in Sec. 5.
Many groups are today able to manufacture SHJ solar cells with efficiencies exceeding 20%, and $V_{oc}$s well above 700 mV. However, since the rediscovery of the SHJ concept in the 1990s, and the introduction of the i-a-Si:H buffer layer, the record in SHJ cell efficiency has been held by Sanyo, now Panasonic. The currently best double-sided SHJ cell has an efficiency of 24.7% ($V_{oc} = 750$ mV, $J_{sc} = 39.5$ mA/cm$^2$, fill factor = 83.2%) [248]. The cell was fabricated from a 98µm thin wafer on an area of 100cm$^2$. With this step, the HIT cell not only surpasses the best published result for a large area production type cell, i.e. SunPower’s 24.2% efficient rear contact cell [178], but falls short by only 0.3% of the PERL cell manufactured by UNSW that holds the world record for a c-Si solar cell and is fabricated on a small area (4cm$^2$), with photolithographic processes that are incompatible with large-scale, low-cost industrial production. It is interesting to note that the improvement over Sanyo’s previous 23.7% cell stems mainly from an improved fill factor, which went up by 2.3% as compared to the previous best cell. With a fill factor of 83.2%, the HIT cell has now indeed closed the fill factor gap that was (and, for other groups working in the field, still is) present between highest efficiency homojunction and heterojunction solar cells [303]. Furthermore, the high $V_{oc}$ of Sanyo/Panasonic’s cell is also related to the low wafer thickness. For solar cells with excellently passivated surfaces, the total (wafer thickness integrated) density of recombination-active states is dominated by the c-Si bulk recombination centers, thus scales with wafer thickness. Therefore, the photogenerated charge carrier density, thus the $V_{oc}$, increases until the wafer is too thin to absorb the incoming sunlight sufficiently well. Therefore, the theoretical maximum $V_{oc}$ peaks at 769mV for 100µm wafer thickness [307], a value that Sanyo has come surprisingly close to.

Further remarkable high-efficiencies reported by the Institute of Microengineering (IMT) at Ecole Polytechnique Fédérale de Lausanne (EPFL), for SHJ cells based on n-type and p-
type c-Si wafers [263] are 22.1% and 21.4%, respectively. To our knowledge, the latter is the
highest reported for a SHJ cell on p-type wafers.

Regarding highly efficient cells on large area and industrialization of the SHJ concept,
Sanyo/Panasonic have shown above 21% cell efficiency (>18% module efficiency) in
industrial production [249]. The French Institut National de l’Énergie Solaire (INES) has
reported 21% and 22.2% efficient cells on 103cm² made with Ag screen-printed and Cu
plated contacts, respectively [259], and Roth&Rau/Meyer Burger have shown large area (6”)
cells with 21.3% efficiency [308]. Very recently, Choshu industry has reported a 24.1%
efficient SHJ cell on an area of 243.4cm², which features cerium oxide and hydrogen co-
doped indium oxide films as TCOs [309]. Further important steps to lowering the levelized
cost of energy are Roth&Rau’s 21.6% efficient cell on a 239 cm² pseudosquare Cz wafer
with a Ag-free front grid, cells above 21% efficiency on a pilot line equipment and their
demonstration of a 303W SHJ module made of sixty 6” pseudosquare SHJ cells [310]. A
production line with a throughput of 4800 wafers/h and a target efficiency of 21% is also
available.

Si heterojunctions have also been used in hybrid cell concepts, i.e. cells where only one of
the junctions is formed as a SHJ. An example of this concept is an inverted SHJ hybrid cell,
where in addition, the p-n junction is located on the rear of the cell instead of the front side
that is facing the sun. With a rear side SHJ (i.e. back heterojunction) in combination with a
diffused (thus, homojunction) front surface field and point contacts on the front, a cell
efficiency of 22.8% has been reported [311].

Another hybrid concept is pursued by Hekmatshoar et al. who introduce a thin, highly
doped epitaxial c-Si film between the c-Si wafer and an a-Si:H on one side, and an a-Si:H
heterojunction with an additional a-Ge:H interlayer on the rear, leading to a 21.4% efficient
cell [312].
4.8 Future direction

Given the rapid progress discussed, it is very likely that c-Si wafer based SHJ technology will approach the 25% cell level efficiency in production. However, there remain many challenges for further improving SHJ cell technology. For example, in order to improve $J_{sc}$, better transparency of the contact layers is needed. For the a-Si:H films, this might lead to their substitution by microcrystalline Si (µc-Si:H), amorphous Si oxide (a-SiO$_x$:H) or amorphous Si carbide (a-SiC$_x$:H) films. TCOs with increased transparency/carrier mobility could be based on hydrogen doped In$_2$O$_3$, or alloys of indium and oxygen with other metals [309]. For the TCO, the indium cost issue might be solved by its substitution, e.g. by ZnO:Al, although the problem of an unsuitable work function/parasitic diode on p-a-Si:H needs to be solved, probably by TCO/a-Si:H interface engineering (by insertion of suitable interlayers).

Another cost driver is the high amount of Ag used in screen-printed contacts. This has already led to approaches using electroplating. However, their long-term reliability is as yet unproven. Looking further into the future of c-Si based PV, it is clear that SHJ are an ideal technology not only for fabricating cells on ever thinner wafers, but also for innovative approaches based on high quality wafer-like thin-film Si solar cells on glass. In this case, the key feature of the SHJ technology is that process temperatures stay below 200°C at all times, i.e. far below the melting temperature of the glass. Promising results have been demonstrated for SHJ on kerf-loss free Si thin-films transferred to a glass carrier [313], and also for a-Si:H/poly-Si cells (Fig. 37), where a ~10 μm thin Si film is deposited onto the glass with high rate e-beam evaporation, then recrystallized by scanning with a line-shaped electron or laser beam. This yields a polycrystalline Si film with grain sizes up to a cm$^2$ [314].
Fig. 37 Schematic cell design of the Front ERA (front contacted electron beam recrystallized absorber) a-Si:H/poly-Si heterojunction solar cell on glass. The poly-Si absorber is a ~10μm polycrystalline Si thin-film consisting of grains with a width in the mm range, and up to several cm long. Polycrystalline Si thin-film is deposited by e-beam evaporation with high deposition rate, and then recrystallized by electron or laser beam. Reproduced from [314], Haschke, J. and Jogschies, L. and Amkreutz, D. and Korte, L. and Rech, B. Polycrystalline silicon heterojunction thin-film solar cells on glass exhibiting 582mV open-circuit voltage, Solar Energy Materials & Solar Cells, 115 (2013) 7. Copyright © 2014 Elsevier B.V. License number 3472100659635.

Furthermore, their high-efficiency makes SHJ cells (and other high-efficiency c-Si based solar cells concepts) a very interesting candidate for combining them with wide bandgap cells into double-junction solar cells, which have the potential to break the efficiency limit of single-junction solar cells. Combinations of III-V based top cells with c-Si cells are discussed in Sec.6. However, due to the thermal constraints, the combination of III-V with SHJ cells is difficult. An alternative approach that has recently drawn much attention are metal halide perovskite-based top cells (see Sec. 10), which can be combined with SHJ cells in either monolithically integrated 2-terminal devices [315, 316, 317] or by mechanical stacking of the two sub-cells, leading to a 4-terminal device, where each subcell has its own electrical connection. For the monolithically integrated 2-terminal devices, efficiencies have reached 21.4% [315]. For the 4-terminal cells, efficiencies between 13 and 22.8% have been reported [318, 319,320].

The development of compatible processes and, importantly, semi transparent contact systems for the perovskite top cells are currently an important field of research, with different approaches ranging from sputtered TCOs to solution processed layers such as Ag nanowires
Furthermore, it has been recognized that tuning of the perovskite top cell’s bandgap to an optimum value of around 1.74eV will allow for further improvements of double-junction cell efficiency. Recently, it was experimentally shown that a photostable perovskite based on mixtures of cesium and formamidinium as well as mixed iodide and bromine can be employed to tune the bandgap to 1.74eV enabling a high $V_{oc}$ of 1.2eV [322].

5.0 Crystalline Si based solar cells: back heterojunction

A reasonable estimate for the technologically achievable efficiency limit of single-junction c-Si based solar cells is about 28% ($J_{sc} = 42.5\text{mA/cm}^2$, $V_{oc} = 760\text{mV}$, fill factor = 87%) [323]. To approach the theoretical efficiency limit in Si based solar cell [307], several strategies can be explored. One of the most attractive technologies is the IBC cell structure. Here, as mentioned in Sec.3, both cell electrodes are located on the rear side of the solar cell and laid out as two interdigitated combs. If the front surface recombination processes have been reduced, this approach overcomes the main limitation to the $J_{sc}$ of the cell imposed by the front grid shaped contact shadowing. The shadowing is about 8% of the cell area and can be reduced to 4% using relatively sophisticated and expensive techniques [76]. In the IBC structure the front side of the cell is completely exposed to the sun to maximize light absorption when an appropriate anti-reflection coating is deposited on the device surface. IBC concept, initially proposed by Lammert and Schwartz [183], is the most relevant feature of the SunPower solar cell that achieved a record efficiency of 24.2% on n-type Fz c-Si wafer [178]. Here, the choice of Si heterojunction, instead of high-temperature emitter diffusion to form a homojunction, has demonstrated several advantages, such as: (i) high $V_{oc}$ due to the potentiality of SHJ and due to the good c-Si surface passivation promoted by the a-Si:H layer that reflects in high cell efficiency as demonstrated by several groups as listed in Ref.[324]. Even though the SunPower homojunction record efficiency cell reaches a $V_{oc}$ value of 720 mV, the highest $V_{oc}$ value of 750 mV, as well as cell efficiency of 24.7% on c-Si based
101.8 cm$^2$ solar cell have been recently demonstrated by Sanyo-Panasonic heterojunction HIT cell [325]; (ii) excellent stability since the extremely thin a-Si:H layer used in the HJ technology is not prone to the undesired Staebler-Wronski degradation effect [326] that still affects the a-Si:H thin-film solar cells; (iii) lower voltage reduction under thermal stress during sunlight exposure with respect to conventional c-Si based cells (-0.3%/°C vs -0.5%/°C). This represents a great advantage in operating conditions since the cells are packaged using glass and plastic and left under sunlight with low possibility to dissipate the thermal excess; (iv) lower cell manufacturing cost due to reduced process time and to lower thermal budget in the cell fabrication. The last allows the use of very thin c-Si wafer [327] that can strongly reduce the photovoltaic cost [29,328].

By merging the SHJ and IBC concepts it is possible to realize a promising technology for c-Si solar cell [329]. In this section, relevant issues of IBC-SHJ (i.e. back heterojunction) design for solar cell fabrication will be discussed and the industrial perspective of this cell concept will be also be discussed.

5.1 Brief history and status of art

The idea to apply the IBC concept to the HJ cell, to take advantage of low thermal budget process and high $V_{oc}$ together with a fully exposed sunward side, was proposed by Lu et al. [330]. They developed cells based on polished 2.5 Ω-cm n-type c-Si Fz 300 μm thick wafer. Both 20 nm thick each p-type a-Si:H emitter and n-type a-Si:H base contact were deposited in a multi-chamber PECVD system at temperature of 200°C at the rear side of the cell to form an interdigitated structure, by photolithography, consisting of 1.2 mm wide strips for emitter and 0.5 mm for base contact, separated by 2 μm wide non-diffused and non-passivated region. The sunward side was passivated by 20 nm intrinsic a-Si:H layer, subsequently covered with ITO and magnesium fluoride double layer as ARC. In subsequent publication [331] the same group of authors demonstrated the role of Si surface passivation
between the doped regions to achieve higher cell efficiency. Tucci et al. presented a novel scheme for heterojunction called **Back Enhanced Heterostructure with INterDigitated** (BEHIND) contact solar cell [332-334]. This method neither involved wet chemical steps, nor photolithography to pattern the two interdigitated back contacts. They were deposited by PECVD as a comb shape with the help of metallic masks, self-mechanically aligned in a specifically designed holder for both the c-Si wafer and the masks. In principle this method may easily be scaled up for large area cells, appropriate for industrial applications. The BEHIND solar cells were fabricated on 200µm thick, <100>, 1 Ω-cm p-type, Cz c-Si wafer.

After front side alkaline texturing and RCA cleaning, a double layer stack of a-Si:H/SiN was deposited on the sunward side, acting as passivation and anti-reflection layer [335]. Then on the whole polished wafer backside, after a short 2% HF procedure to remove the native oxide, an intrinsic a-Si:H buffer layer was deposited before the n-type a-Si:H emitter. To increase the emitter conductivity a chromium silicide (CrSi) layer was then formed [336] by chromium (Cr) evaporation and wet chemical removal. A metallic mask, fabricated from a 100µm thick molybdenum foil having a comb shaped aperture, was fixed over the emitter layer. A dry etching procedure using nitrogen trifluoride gas was performed to remove the n-type a-Si:H portion not covered by the mask, using settings defined on the base of previous experiments [337]. Subsequently, keeping the mask in the same position, the cell base contact was formed by an intrinsic a-Si:H buffer and a p-type a-Si:H layers. Through the same mask, a 30nm thick Cr layer was evaporated. Then a low-temperature sintering Ag paste was screen-printed on both interdigitated contacts [338]. The BEHIND cell was the first IBC-BHJ (Fig. 38) cell fabricated without any photolithographic step and it demonstrated the possibility to deposit a-Si:H film through metal masks. The total area of the solar cell was 6.25cm². Different versions of the cell process were presented in literature and the best results
are reported in Table 1. Schematic diagram of IBC-BHJ cell is shown in Fig. 38. Here, n-type c-Si, p-type a-Si:H and n-type a-Si:H acts as base, emitter and BSF respectively.

![Schematic diagram of IBC-BHJ cell](image)

Fig. 38 Schematic diagram of IBC-BHJ cell showing grid-less front surface. Neglecting the recombination at front and rear c-Si surface, when charge carriers are photogenerated within the c-Si wafer, due to concentration gradient, charge carriers diffuse to the rear side of the cell where they can be collected by their respective electrodes if charge carriers are able to arrive in the depletion region formed close to the p-type a-Si:H emitter layer. Therefore, in principle, the distance between two emitter regions should be thinner than half of minority carrier diffusion length. Photogenerated electrons can be collected in the n-type a-Si:H contact if able to overcome the intrinsic a-Si:H passivation layer. BHJ design eliminates shadowing effect caused by metal grids and allows sufficient metal to be used at the rear side to minimize resistive losses.

In early 2011, Helmholtz-Zentrum Berlin (HZB) together with Institute for Solar Energy Research Hamelin (ISFH) group developed a 20.2% efficient IBC-BHJ cell [232] on n-type 3Ω-cm Fz wafer. The front side was textured and phosphorous diffused to form a front surface field, and then passivated by SiO2/SiN. The back side area was covered by 60% emitter contacts (p-type), 28% base contact (n-type) and 12% gap space between these, passivated by a SiO2/SiN stack, with pitch in the range of millimetres. The metal contact was Al for both emitter and base regions. Two different approaches were considered: with or without intrinsic buffer layer just under the emitter, obtaining in both cases nearly 20% efficiency. In the first case $V_{oc}$ is 40mV higher (673mV), but the fill factor is nearly 3% absolute lower (75.7%); due to the $J_{sc}$ (39.7mA/cm²) the efficiency was 20.2%. Without buffer layer the $V_{oc}$ was 633mV but the fill factor was as high as 78.8% with the same
current, so that the efficiency was 19.8%. The entire cell fabrication process was performed on 1cm² area by photolithographic steps. The best results are summarized in Table 1.

The participants of the SHARCC project in France developed an innovative process called SLASH (Structuring by Laser Ablation of Si Heterojunction). They suggested the following sequence of steps: (i) emitter deposition and patterning by laser ablation; (ii) base contact deposition and laser patterning; (iii) front ARC deposition; (iv) ITO deposition; (v) screen-printing at low-temperature; (vi) laser ablation to separate the contacts. With this technology a 19% efficiency (Table 1) on 25 cm² area has been demonstrated [259,339].

The IBC-BHJ proposed by IMEC Belgium started from Cz n-type, 3-4Ω-cm <100> c-Si wafer with thickness of either 150 or 280μm. Different front side passivation schemes were adopted: n⁺-diffusion (POCl₃) and HJ on both textured and flat surface. Then on the rear side of the wafer a i-a-Si:H passivation layer, and p⁺-doped emitter were deposited by PECVD at temperatures less than 200°C. An ITO transparent conductive oxide was deposited on the a-Si:H layers. Photoresist was spun on both sides of the wafer, and patterned on the rear side, before etching through the ITO. Openings through the a-Si:H layer were performed by wet chemical etch. After HF dip, Al base contacts were deposited by e-beam evaporation. The emitter contact was obtained by depositing Ti/Pd/Ag using e-beam evaporation on the ITO layer using shadow masks. A final anneal was performed in nitrogen at low-temperature. An efficiency of 15.2% efficiency was achieved on 1cm² area [340]. The best results are summarized in Table 1.

The BACH (Back Amorphous-Crystalline Si Heterojunction) cell was developed at University of Toronto. The cell was fabricated on n-type 300μm thick 20 Ω-cm Fz c-Si wafer. In this case the fabrication process consisted of different photolithographic steps with at least 4 photomasks. The process sequence also included initial oxidation of the n-type wafer to have surface passivation, and electrical isolation between emitter and base contacts.
at the back side. The front surface was textured. The efficiency of IBC-BHJ cells with an area
of circa 1cm² was of 16.7%, with \( V_{oc} \) of 641mV, and \( J_{sc} \) of 33.7mA/cm². However fill factor
was appreciably higher than 77% [341,342]. The major limiting factor for both \( V_{oc} \) and \( J_{sc} \)
was recognized due to surfaces passivation.

The latest design is by LG Electronics. However very few details are available on the
technology adopted. The design started on n-type Cz and Fz c-Si. After texturing, n-a-
Si:H/ARC films were deposited for FSF front surface passivation. Then on the wafer rear
side, n-type a-Si:H base and p-type a-Si:H emitter were deposited. On both doped regions the
TCO was deposited and subsequently an Ag metal contact was screen printed, or Cu
electrodes were electroplated [343]. In February 2014 Panasonic company announced
efficiency higher than 25% [344] on very large area device as reported in Table 1, in which
all the best results are reported.

Table 1 List of PV parameters of the IBC-BHJ cells.

<table>
<thead>
<tr>
<th>Institution</th>
<th>( V_{oc} ) (mV)</th>
<th>( J_{sc} ) (mA/cm²)</th>
<th>Fill factor (%)</th>
<th>Area (cm²)</th>
<th>c-Si wafer</th>
<th>Patterning</th>
<th>Metallization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Panasonic</td>
<td>740</td>
<td>41.82</td>
<td>82.7</td>
<td>25.57</td>
<td>143.7</td>
<td>n-type</td>
<td>-</td>
</tr>
<tr>
<td>LG Electronics</td>
<td>723</td>
<td>41.8</td>
<td>77.4</td>
<td>23.4</td>
<td>4</td>
<td>n-type Fz</td>
<td>Sputtered Al</td>
</tr>
<tr>
<td></td>
<td>692</td>
<td>38.4</td>
<td>77.9</td>
<td>20.7</td>
<td>238.95</td>
<td>n-type Cz</td>
<td>Screen Printing</td>
</tr>
<tr>
<td></td>
<td>716</td>
<td>37.5</td>
<td>76.4</td>
<td>20.5</td>
<td>238.95</td>
<td>n-type Cz</td>
<td>Electroplated Cu</td>
</tr>
<tr>
<td>HZB</td>
<td>673</td>
<td>39.7</td>
<td>75.7</td>
<td>20.2</td>
<td>1</td>
<td>n-type 3 ( \Omega )-cm Fz</td>
<td>Photolithog.</td>
</tr>
<tr>
<td>INES-CEA</td>
<td>695</td>
<td>36.6</td>
<td>75.2</td>
<td>19</td>
<td>25</td>
<td>n-type 1-5 ( \Omega )-cm Fz</td>
<td>Evaporated Al</td>
</tr>
<tr>
<td>University of Toronto</td>
<td>641</td>
<td>33.7</td>
<td>77.3</td>
<td>16.7</td>
<td>1</td>
<td>n-type 1 ( \Omega )-cm</td>
<td>Photolithog.</td>
</tr>
<tr>
<td>IMEC</td>
<td>605</td>
<td>39.1</td>
<td>64</td>
<td>15.1</td>
<td>1</td>
<td>n-type 1-4 ( \Omega )-cm</td>
<td>Photolithog.</td>
</tr>
<tr>
<td>ENEA</td>
<td>695</td>
<td>35.3</td>
<td>60.9</td>
<td>15</td>
<td>6.25</td>
<td>p-type 1 ( \Omega )-cm</td>
<td>Shadow mask</td>
</tr>
<tr>
<td>University of Delaware</td>
<td>602</td>
<td>26.7</td>
<td>73</td>
<td>11.8</td>
<td>1.32</td>
<td>n-type 2.5 ( \Omega )-cm</td>
<td>Photolithog.</td>
</tr>
</tbody>
</table>

5.2 Interdigitated back contact design

Several aspects of the device design are needed to be carefully accounted for to achieve
high-efficiency solar cell. One of them is, for example, is having minority-carrier lifetime
corresponding to diffusion length at least three times higher than the wafer thickness.
Moreover other parameters have to be rightly addressed to design the highest efficiency solar
cell. In this section the choice of materials and the design aspects needed to optimize the IBC-BHJ cell are reviewed.

5.2.1 Choice of c-Si wafer

The choice of wafer type and doping level play a dominant role in device design due to the asymmetry of material properties respect to the carriers. Some considerations from physics, chemistry, and industrial engineering can drive that choice but sometime in opposite directions. Physically, p-type c-Si should be used in IBC solar cell since the minority photogenerated carriers move by diffusion and, when p-type is chosen, minority-carriers are electrons with lower effective mass and higher mobility than holes [341]. On the other hand n-type c-Si should be preferred to avoid boron-oxygen undesired complex formation, which is responsible for efficiency degradation under sunlight exposure [345]. The best HJ cell efficiency was demonstrated on n-type c-Si [327] due to useful band alignment at the both front and rear interfaces [346], as evident from the upper side of Fig. 39. The asymmetry in the offset displacement between a-Si:H and c-Si, higher in valence band than in conduction band [287], plays a role in the device design. It is not a serious problem for the main p-n junction due to the electric field arising from the junction built-in potential, but it introduces a difficulty for the base contact [347]. Band distributions, as deduced from numerical simulations [348] of HJ device based on the two different doping types of c-Si wafers, are compared in Fig. 39. The n-type c-Si/n-type a-Si:H contact forms an Ohmic contact and a spontaneous BSF helpful to keep holes away from the base metal electrode. The p-type c-Si/p-type a-Si:H contact needs some care to ensure the majority carriers collection with reduced probability of recombination at the base metal electrode. A comparison of I-V characteristics of HJ base contacts of devices based on p-type or n-type c-Si wafer is shown in Fig. 40, as deduced from numerical simulations (solid lines) performed on different a-Si:H layer thicknesses and experimental results (symbols). By comparing experiment and the
simulation results, the perfect Ohmic behaviour of n-c-Si/i-a-Si:H/n-a-Si:H heterostructure is evident. In case of p-type c-Si, a p⁺-layer is needed to approach the Ohmic characteristic as that obtainable using Al diffusion into p-type c-Si, shown in Fig. 40 as red symbols and solid lines. A density of states of 1x10¹⁵/cm³/eV within intrinsic a-Si:H layer has been used in performing the simulations.

![Band diagram comparison of HJ structure based on n-type c-Si wafer (upper side) and p-type c-Si wafer (lower side) as deduced from numerical simulations. The light impinges the heterostructure on the left side. Electrons (red dots) can easily cross the small band offset at the p-c-Si/n-a-Si:H interface as well as at n-c-Si/n-a-Si:H. Holes (blue dots) cross the n-c-Si/p-a-Si:H interface with the aid of electric field, but can be reflected at the p-c-Si/p-a-Si:H interface due to the large valence band offset between c-Si and a-Si:H materials. Note that band offset is higher in the valence band than in the conduction band, plays a role in the device design. Both Ohmic contact and a spontaneous BSF is formed between n-type c-Si/n-type a-Si:H and keeps holes away from reaching the metal electrode.](image)

![I-V characteristics in dark conditions of heterojunctions based on p-type and n-type c-Si wafer. Experimental data (exp.) and simulations (sim.) are reported as symbols and solid lines respectively. A perfect](image)
Ohmic contact can be seen for the n-c-Si/i-a-Si:H/n-a-Si:H heterostructure (green dots and curve). For p-c-Si, a p⁺-layer is required for Ohmic contact which can be obtained by Al diffusion into p-c-Si (red dots and curve). Thicknesses and doping of a-Si:H films are relevant to achieve a properly working contact at p-c-Si/p-a-Si:H interface. The n-c-Si/n-a-Si:H is less critical, while the p-c-Si/p-a-Si:H contact needs particular care. Indeed only high doping values of p-a-Si:H layer can avoid a barrier formation against carrier transport, as evident comparing the blue dots and curve with the black ones.

Wafer doping and bulk lifetime play a role in interdigitated contact geometry as demonstrated by two dimensional numerical simulations of the IBC-BHJ device reported in [349], in which p-type c-Si wafer is adopted. As expected, $J_{sc}$ reduces from 37mA/cm² by increasing the doping concentration from 10Ω-cm to 0.1Ω-cm due to bulk lifetime degradation in highly doped regions, where Auger mechanism dominates the recombination process. At the same time fill factor increases due to reduced bulk series resistance.

Figure 41 shows the effect of doping concentration on fill factor and cell efficiency for different bulk lifetime, taking into account a textured surface for the c-Si. In these simulations, the distance between the doped a-Si:H regions has been fixed at 100µm, and a p-type c-Si doping density of $5 \times 10^{16}$/cm³ (0.5Ω-cm) should be preferred [330].

![Graphs showing the effect of doping concentration on fill factor and cell efficiency](image)

**5.2.2 a-Si:H doping**
Another asymmetry to be considered in device design is due to the difference between doping effectiveness of n- and p-type a-Si:H material. N-type (p-type) doping, obtainable by adding PH₃ (B₂H₆) to the SiH₄ in PECVD chamber during the plasma, ensures higher film conductivity and lower activation energy. In Fig. 42, activation energy and conductivities of p-and n-type a-Si:H films are reported as a function of dopant concentration in the gas mixture during the PECVD process [350]. Unfortunately, in doped a-Si:H thin layer, the thinner the film the higher the activation energy [351]. Therefore the choice of any emitter thickness should be carefully considered and verified to correctly design an IBC-BHJ solar cell.

![Graph](image)

Fig. 42 Left side: Dark conductivity and activation energy (Eₜ) of n-a-Si:H films versus phosphine (PH₃) content in the gas mixture during the film growth by PECVD. Right side: Dark conductivity and activation energy of p-a-Si:H films versus diborane (B₂H₆) content in the gas mixture during the film growth by PECVD. For both types of dopants, by increasing dopant concentration, activation energy decreases and conductivity increases. High film conductivity and low activation energy are required. Note that, thinner the film, higher the activation energy. In BHJ solar cells, doped a-Si:H is used as emitter. Therefore, to design BHJ solar cell, emitter thickness should be carefully chosen.

To improve the electrical properties of n-type a-Si:H layer, a chrome silicon (CrSi) formation on top of the amorphous film was suggested [336]. This CrSi can be obtained by depositing 30nm of Cr on doped a-Si:H and patterning it by wet chemical etch in a solution of 30g of cerium ammonium nitrate ((NH₄)₂Ce(NO₃)₆), 9ml CH₃COOH and 200ml of DI water. Activation energy reduction from 0.24eV down to 0.017eV was obtained. CrSi can also be useful in the case of p-type a-Si:H. Indeed the presence of the CrSi layer does not
affect the doping type of the doped a-Si:H film on which it is formed. Activation energy
reduction from 0.36eV down to 0.14eV has been achieved [336]. This treatment improves the
p-c-Si/i-a-Si:H/p-a-Si:H/p⁺-a-Si:H heterojunction contact to form an effective ohmic contact,
as shown in Fig. 40 [347]. Since both contacts are on the rear side of the cell the energy gap
of the a-Si:H becomes less relevant. The a-Si:H film on the rear side does not work as a
window layer. Therefore lower bandgap should be preferable in order to reduce the valence
band offset at a-Si:H/c-Si interface, thus enhancing the charge collection as in the case of µc-
Si:H cell [352]. Nevertheless the buffer layer should continue to be amorphous for better
passivation of c-Si surface. On the other hand higher bandgap materials must be avoided as
suggested in Ref. [13], otherwise the energy mismatch between the two valence bands at the
heterojunction produces a high barrier that cannot be overcome by the electric field.

5.2.3 Buffer layer - Intrinsic a-Si:H

It is widely accepted that an effective heterojunction must have intrinsic, high quality
a-Si:H buffer layer to passivate the c-Si surface and to separate the doped a-Si:H film
[325,353]. Its thickness must be carefully optimized taking into account of the monohydrides
(Si-H), dihydrides (Si-H₂) content at the beginning of the a-Si:H film deposition to avoid
epitaxial growth [354]. Potential for further improvements are still under investigation to
reduce the SRV [278, 355]. In the case of IBC-BHJ device, depending upon the patterning
processes, the situation is more complex since the buffer layer should be the same for both
base and emitter contacts. Two dimensional numerical simulations have been used to
evaluate the effect of the buffer layer thickness. In Ref.[338] it is reported that increasing the
i-a-Si:H buffer layer thickness, the light I-V characteristics under standard AM1.5G (G stands
for global) condition are strongly affected resulting in a fill factor reduction. In the simulation
a defect density of 10¹⁷/cm³/eV is homogeneously distributed along the buffer layer thickness.
This effect is related to the recombination at the a-Si:H/c-Si interface. Indeed when the i-a-
Si:H layer becomes thicker, the p-type a-Si:H base contact is not able to collect the holes due to the valence band offset at the edge of a-Si:H/c-Si interface. These holes recombine through a-Si:H/c-Si interface defects, with electrons generated in the c-Si bulk and diffusing toward the n-type contact. This results in a barrier formation against carrier collection from the base contact. This recombination produces an S-shape in the I-V curve, such as coming from an anti-series double diode device. The simulated band bending at the edge of c-Si/i-a-Si:H/p-a-Si:H is already shown in Fig. 39. Of course the intrinsic layer cannot be completely removed otherwise the c-Si surface passivation in the region not covered by doped a-Si:H layer will be immediately lost [232]. However in IBC-BHJ, the c-Si rear side surface passivation is not the same as in the case of SHJ (i.e. front heterojunction) emitter. Indeed now the emitter region partially covers the buffer layer on the c-Si surface, while the other part is covered by the base contact HJ. A gap region between base and emitter contact also has to be considered, as evident from Fig. 38. This difference between SHJ and IBC-BHJ in surface passivation accounts for only ~ 2% of the fill factor change [234]. Moreover the higher the defect density within the buffer layer the stronger the undesired S-shape effect even for a relatively thin buffer layer.

The thickness of the intrinsic a-Si:H buffer layer is also important for consideration or improved performance. The thicker the buffer layer, the lower the cell fill factor as shown in Fig. 43. Increasing the buffer layer thickness from 3.5nm up to 14nm, a S-shape appears in the I-V characteristic. Further details concerning the two dimensional simulations shown in Fig. 43 can be found in Ref. [338].
Fig. 43 Simulated I-V curves as a function of intrinsic a-Si:H buffer layer thickness. By increasing buffer layer thickness from 3.5 nm up to 14 nm, an S-shape appears in the I-V characteristic. This effect refers to a barrier formation against carrier collections that forms at the heterojunction interface. Therefore very thin buffer layer should be adopted to obtain a proper working heterojunction device. On the other hand, buffer layer thickness should not be further reduced otherwise it is very difficult to ensure a conformal coverage of Si surface. Moreover buffer layer thinner than 5 nm does not represent a good choice. Indeed if this buffer is too thin, less than 5 nm, surface passivation cannot be guaranteed, due to higher content of dihydrides (Si-H₂) radicals at the interface between c-Si and a-Si:H. A 5-7 nm thick buffer layer represents the best choice for practical use.

5.2.4 Metal contacts

The low conductivity of doped a-Si:H layer has a strong impact on IBC HJ cell. If the emitter region is not completely covered by any metal contact, the carriers have to travel laterally along the doped a-Si:H film to reach the metal electrode. The longer distance for lateral transport introduces resistance loss that results in fill factor reduction, whereas $V_{oc}$ and $J_{sc}$ are not affected by the reduction of the metal coverage. Numerical simulations of IBC-BHJ device reported in Ref. [349] show that decreasing the coverage ratio from 100% to 50% induces an absolute 5% reduction of fill factor, thus reducing the cell efficiency. Therefore the whole emitter area has to be contacted by a metal to achieve the best cell performance.

Concerning the emitter coverage, the use of TCO represents a good choice to improve the lateral conductivity of the very low doped a-Si:H layers. This is because CrSi may not be sufficient to guarantee a sufficient lateral conduction if the metal contact is narrower than the emitter region.

The challenge of TCO patterning without any photolithography processes remains. Up to now the most promising technologies are the use of physical shadow mask during the
sputtering process [338, 340] and the laser ablation after TCO deposition [339].

The choice of the electrodes deposited on both contacts represents another relevant issue. Indeed the electrode work function can affect the doped a-Si:H layer conductivity. In principle the n-type a-Si:H should be sufficiently thin to avoid series resistance enhancement and sufficiently doped to avoid depletion induced by the electrode contact due to the work functions not aligning within the a-Si:H layer. As an example, if the Fermi level assumes a distance of 4.2eV from the vacuum level to the edge of n-type a-Si:H emitter, work function of the electrode should not exceed that value to avoid depletion in the a-Si:H layer when in contact with that electrode, otherwise a Schottky barrier contact arises. This again deforms the light I-V characteristics introducing a S-shape.

A comparison of band bending distributions at the rear side of the cell is reported in Fig. 44, as obtained by numerical simulations. Here two different work function values of 4.3 eV (black for Al), and 4.6 eV (Red for TCO) have been applied as rear side metal contact of a n-c-Si/i-a-Si:H/n-a-Si:H heterostructure, keeping the same doping and density of state distribution within the n-type a-Si:H layer. The work function were simulated by fixing the Fermi level at the edge of the n-a-Si:H layer where the metal contact would be. As evident from Fig. 44, a depletion occurs in both n-type c-Si and a-Si:H that reflects in a barrier formation for the electrons being collected by the metal contact. This barrier results again in a S-shape in the light I-V characteristic as reported in Fig. 44 as continuous lines and compared for two different cells. The metal electrode has been varied from Al (work function = 4.3eV) to TCO (work function = 4.6eV). Also on the p-type a-Si:H layer an undesired depletion effect can be obtained if an uncorrected metal work function is chosen.
Fig. 44 Left side: Numerical simulations of band bending distributions of n-c-Si/i-a-Si:H/n-a-Si:H rear side of heterojunction solar cell, in which the work function of the metal contact to the n-a-Si:H has been varied from 4.3 eV (black for Al) to 4.6 eV (red for TCO). Moreover black lines in the band diagram shifted a bit downward due to an electron accumulation (inside the barrier) induced by the metal work function. The barrier formation results in a S-shape light I-V curve (right side) reported as continuous lines; Right side: Comparison between experimental (dots) and numerically simulated (line) I-V characteristics under sun-light illumination of n-c-Si/n-a-Si:H rear side of heterojunction solar cell in which the work function of the metal contact to the n-a-Si:H has been varied from TCO = 4.6eV (red) to Al = 4.3eV (black).

To reach the highest efficiency, metal work function close to 4.3eV and 5.2eV should be used in case of n- and p-type a-Si:H regions, respectively [346]. According to this approach the built-in voltage of the device also can increase leading to higher V_{oc} values [327]. Band bending simulation of the n-type c-Si based a-Si:H/c-Si heterojunction cell with two different metals work function (5.2eV and 4.3eV) for the emitter and base contact respectively is shown in Fig. 45. This simulation refers to a HJ device able to reach V_{oc} of 760mV and efficiency of 25%. At the left side the band bending at the edge between metal and p-type a-Si:H is magnified to remark the undesired band bending distribution when metal work function lower than 5.2eV is used for the contact.
Fig. 45 Band bending simulation of the n-type c-Si based a-Si:H/c-Si heterojunction cell. This simulation is for heterojunction device with $V_{oc}$ and efficiency of 760mV and 25% respectively. Two different metals with work function ($W_f$) of 5.2 eV and 4.3 eV are adopted for the emitter and base contact respectively. These metals have the same effect of TCO films from the work function point of view. For small area (lab scale) devices, metal work function is not an issue. At the left side, the band bending at the edge between metal and p-type a-Si:H is magnified to illustrate the undesired band bending distribution when metal work function lower than 5.2 eV is used for the contact. Here, electron affinity and Fermi energy are denoted by $E_f$ and $\chi$ respectively.

While at lab scale metal work function does not represent a problem, since different metals are commonly available and small area samples requires thin layers, the situation become more complex when production moves to industrial scale. Thicker layer due to large area device and low-cost metallization processes are needed to be competitive. Towards this, it is useful to look at the front heterojunction cell manufacturing process where the device commonly has two TCO for both front and rear side of the cell. TCO layers are usually obtained by magnetron sputtering, which is a standard technology for large area solar cell. Even if the TCO is also useful to work as anti-reflection coating, its resistivity around $10^4 \Omega$-cm is not sufficient to ensure lateral collection without introducing series resistance. Then Ag metal grids are needed to complete the cell. This metal is commonly using through screen printing process with thermal sintering at temperature below 200°C [346]. This technology can be applicable also to the IBC-BHJ device due to the low thermal budget required.

Several TCOs such as Al-doped ZnO (ZnO:Al) and ITO can fit the work function requirements. In particular ITO can offer the possibility to tune the work function depending
on the deposition conditions [356] as well as the amount of indium within the In$_2$O$_3$ target of
the magnetron sputtering system. A 90% In$_2$O$_3$ and 10% SnO$_2$ result in work function of 5.5
eV and 4.8eV respectively [357]. Moreover in the case of IBC-BHJ device, the TCO
positioned on the rear side of the cell does not work as anti-reflection coating and thus may
be thicker leading to a lower sheet resistance. Nevertheless the rear side contact should also
work as mirror to reflect infrared radiation inward towards the cell, thus enhancing the light
trapping. ZnO:Al/Ag contact represents a better choice with respect to ITO/Ag or Al. ITO or
ZnO:Al also represent a good substrate to Cu plating applications to replace the expensive Ag
layer. In Fig. 46, inward reflectance in the c-Si wafer from different rear side metal contacts
are compared. All these reflectance curves are obtained using optical simulation software
[358]. It is interesting to note that 15nm a-Si:H/Al as back contact does not form an optimum
mirror due to the Al absorption in the wavelength range between 750nm and 1000nm. Cu and
Ag are seen to behave quite similar as mirror in the near infrared portion of the spectrum
between 900nm and 1200nm.

Fig. 46 Inward reflectance in the c-Si wafer from different rear side metal contacts. Al is not the best choice due
to infrared absorption, while Cu and Ag act similar from 900nm to 1200nm. This reflectance is simulated with
the aid of a numerical model developed in x-ray oriented programs (optical simulation software). Red curve
shows that back contact formed by 15nm a-Si:H/Al shows an infrared wavelength absorption. Back contact
should act as mirror, and should reflect infrared wavelength towards bulk. That is, to enhance light trapping, rear
side contact should reflect infrared radiation towards the bulk of c-Si wafer. ZnO:Al/Ag (i.e. AZO/Ag) is a
better choice than ITO/Ag or ITO/Al. Also, Cu plating can be done easily over ZnO:Al. Therefore, an expensive
Ag layer can be replaced easily by Cu.

Contact resistance contributes to series resistance. Contact resistance can be evaluated
with the aid of two-dimensional (2D) numerical model of the IBC-BHJ cell. To achieve cell fill factor as high as 83%, a specific contact resistivity of 0.01\,\Omega\,-\text{cm} for both emitter and BSF contacts should be obtained. Higher contact resistances of 0.1\,\Omega\,-\text{cm} and 1\,\Omega\,-\text{cm} will lead to a fill factor of 80% and 54%, respectively [349]. Higher values of these parameters induce an S-shape in the light I-V sun lighted characteristic.

Different metallization approaches have been proposed on a laboratory scale. According to the previous discussion, industrial production on large area metallization must fit cell cost and throughput. Since the heterojunction cells can only withstand temperatures lower than 300°C, screen printing using low-temperature sintering Ag pastes or metal plating are the only available alternatives. Both these techniques require an interlayer such as TCO [259] or evaporated metal [333] between the doped a-Si:H film and top metal (i.e. Ag paste) to fit the work function requirement, and to ensure metal adhesion.

5.2.5 Distance between doped regions - gap between IBC contacts

In IBC-BHJ cells the primary fill factor loss is due to lateral current flow. Indeed the emitter fingers should be much wider than base fingers for efficient minority-carrier collection; therefore the majority carrier collection is subject to more resistance losses [217]. $J_{sc}$ increases by about 3\,mA/cm$^2$ as the emitter coverage increases from 50% to 95%, because of the increased area. The same effect is also demonstrated in a back-contacted diffused junction solar cell [359]. Fill factor increases along with emitter coverage up to a certain value and then decreases because of the increased series resistance related to the longer travel of the majority carriers to be collected in the base contact, and to the reduced width of the base. To better understand this issue several structures have been simulated having different distance between the two doped a-Si:H contacts. The simulated I-V characteristics in Fig. 47 refer to distance varying between 4\,\mu m to 90\,\mu m. All the other parameters such as SRV, defect density at the interface, and doping density of the doped regions have been kept constant. To
achieve the best efficiency the distance between doped contacts should be as short as possible. Increasing that distance results in a decrease in fill factor. This effect is due to the absence of electric field in crystalline region covered only by the intrinsic a-Si:H layer. The photogenerated carriers flowing into these regions cannot escape from c-Si/a-Si:H interface recombination. Indeed if the density of states in the i-a-Si:H layer were increased by one order of magnitude from $1 \times 10^{17}/\text{cm}^3$, recombination will be stronger and its effect on the I-V characteristic will be dramatic, as evident looking at the dotted black characteristic reported in the Fig. 47 [338]. In practice it is difficult to obtain a distance between the two doped contacts as short as 4 μm without any photolithographic process.

![Fig. 47 Influence of gap distance between the emitter and base contacts and the influence of defect density within the buffer layer. The simulated I-V characteristics refer to distance varying between 4mm to 90mm. All the other parameters such as as SRV, defect density at the interface and doping density of the doped regions have been kept the same for all the simulated distances. To achieve the best efficiency the distance between doped contacts should be as short as possible. Increasing that distance, a reduction of fill factor occurs, due to the reduction of electric field intensity within crystalline region covered by the intrinsic a-St:H layer. If the density of states in the i-a-Si:H layer is increased to an order of magnitude from $1 \times 10^{17}/\text{cm}^3$, the recombination would be stronger and its effect on the I-V characteristic would be dramatic as evident looking at the back dotted I-V curve. Keeping the gap width fixed at 100μm, simulations show that increasing the base contact width, the $J_{sc}$ quadratically decreases from 34 mA/cm² at 100μm down to 30 mA/cm² at 750μm due to recombination at interface n-c-Si/i-a-Si:H/n-a-Si:H, which reduces the number of carriers able to reach the emitter region [349].

To better define the rear side geometry of an IBC-BHJ solar cell, a definition of pitch
as the sum of the base, the gaps and the emitter width, is used. Commonly it is in the millimetres range. From simulations it is possible to determine the optimum pitch, corresponding to the maximum cell efficiency, which is in the range between 600µm and 900 µm. This optimum value is determined as a trade-off between emitter coverage and series resistance losses due to the increased lateral distances. While the pitch weakly influences the Jsc that instead strongly depends on SRV, in turn it affects the fill factor as shown in Fig. 48.

As can be seen in Fig.48, fill factor quadratically decreases as pitch width increases as shown by the parabolic red curve fitting the simulation data. These data refer to simulations in which the base contact and gap widths were set at 150µm and 50µm respectively. Jsc data refers to a SRV of 50cm/s arising from a front surface field [360]. Instead, Mingirulli et al. [232] reported that to achieve the efficiency of 20%, suggests gap, base contact and emitter width in the ratio: 12%, 28% and 60% respectively of the pitch.

![Figure 48](image_url)

**Fig. 48** Fill factor (line) and Jsc (symbols) as a function of pitch width resulting from numerical simulations. Continuous red line shows the quadratic behaviour of the fill factor versus pitch width. In the inset, a sketch of pitch width definition is shown. In the simulation, base width and gap width were set at 150µm and 50µm respectively. By increasing pitch width about an order of magnitude from 250µm, Jsc increased slightly, being weakly influenced by pitch width. Whereas fill factor decreases quadratically as pitch width increases. Jsc data corresponds to a surface recombination velocity of 50cm/s. Maximum efficiency corresponds to a pitch width between 600 and 900µm.

### 5.2.6 Front surface

Since the carriers are mostly generated close to the front side of the cell and the
diffusion mechanism toward the back contact is the only way for the collection, the front side
plays a very relevant role in IBC-BHJ cells. An effective front surface passivation is strongly
needed to reduce the SRV, and achieve high-efficiency. From numerical simulations of IBC-
BHJ solar cell, reported in Ref. [360], it is evident that both $J_{sc}$ and $V_{oc}$ are affected by the
front side SRV. In particular, increasing the SRV from 0 to 1000 cm/s, the $J_{sc}$ and $V_{oc}$ reduce
from 36 mA/cm$^2$ to 15 mA/cm$^2$ and from 760 mV to 660 mV, respectively, thus reducing the
cell efficiency. The fill factor does not seem to be very strongly influenced. An anti-reflection
coating able to ensure low front SRV can be achieved by SiN passivation, or even more
promising, using a-Si:H/SiN stack double layer [335], or SiO$_2$/SiN [232]. A front SRV as low
as 10 cm/s on p-type was demonstrated in Ref. [213, 361]. Moreover SiN deposited on front
side of n-type c-Si surface layer can also form a front surface field due to the electron
accumulation induced by the positive charge lying within the SiN film [362].

In principle the use of a front surface field can be very useful to achieve an effective
surface passivation. In Ref. [213] the impact of the front SRV on the QE of IBC cell has been
demonstrated leading to the conclusion that the SRV affects more the cell fabricated on
higher doped c-Si base. As an example, a $J_{sc}$ of 38.5 mA/cm$^2$ can be achieved for base doping
concentration of $10^{14}$ cm$^{-3}$ even in case of SRV = 40 000 cm/s, whereas the same SRV reduces
the $J_{sc}$ to less than 30 mA/cm$^2$ for base doping concentrations of above $7 \times 10^{15}$ cm$^{-3}$.
Calculations have shown that front surface field on lower base doping results in higher $J_{sc}$ and
reduce the influence of the front SRV [213]. This result is relevant for industrial cell
manufacturing, where good passivation on large areas is still difficult to attain [360]. In
practice it is easier to perform a good passivation on FSF fabricated by light phosphorous
diffusion on n-type c-Si wafer, as suggested in Ref. [232], with respect to light boron
diffusion on p-type c-Si wafer [363]. In turn this approach to the front surface field is in
contrast to the primary goal of achieving a full low-temperature (< 200°C) process able to
reduce the cell manufacturing cost at industrial scale. On the other hand, $J_{sc}$ as high as $38.5 \text{ mA/cm}^2$ have been presented by LG [343] using a n-type a-Si:H/i-a-Si:H front surface field. In this case, however, an undesired absorption within a-Si:H film occurs that reduces the $J_{sc}$ of at least $1 \text{mA/cm}^2$. Therefore the use of higher bandgap n-type thin-film to form an effective front surface field is highly desirable. Doped SiO$_x$ film obtainable by PECVD process [364] can be a valid solution to overcome the undesired absorption at the front side.

The key issue to obtain high $J_{sc}$ depends not only on SRV but also on diffusion length, in the bulk c-Si wafer. The effect of both parameters has been explored in Ref. [333], in which the $J_{sc}$ and $V_{oc}$ of the cell have been simulated by varying the diffusion length and front side SRV, as depicted in Fig. 49. A numerical model based on PC1D software [365] suggests that the front side SRV has a greater effect on device performances than diffusion length. Indeed while a diffusion length of $500 \mu\text{m}$ is acceptable to collect the photogenerated carriers over the entire light spectrum ranging from 350nm to 1200nm, SRV values higher than $100 \text{cm/s}$ strongly decreases the $J_{sc}$ values, thus reducing the advantage of front metal grid absence. To obtain high-efficiency solar cell on a p-type $200 \mu\text{m}$ thick c-Si wafer, the model suggests that SRV as low as $10 \text{cm/s}$ and diffusion length around $1 \text{mm}$ are needed to achieve $J_{sc}$ and $V_{oc}$ values of $38 \text{mA/cm}^2$ and $720 \text{mV}$, respectively. A diffusion length value of $1 \text{mm}$ corresponds to a $300 \mu\text{s}$ of bulk lifetime. To obtain the same diffusion length on n-type doped c-Si wafer, a $1 \text{ms}$ bulk lifetime is required [329] because of lower mobility of holes compared to that of electrons.
Fig. 49 PC1D simulations of $J_{sc}$ and $V_{oc}$ values as a function of diffusion length for different values of front side surface recombination velocity. These values are chosen in the range between 10cm/s and 500 cm/s. While the former refers to very good Si surface passivation, and the latter refers to a surface passivation commonly achieved in the cell production line. Front surface recombination velocity has more influence on device performance than diffusion length, and a high $J_{sc}$ depends on these two parameters. To collect photogenerated carriers over the spectrum range between 350 and 1200nm, a diffusion length of at least 500µm is required. When surface recombination velocity >100cm/s, $J_{sc}$ decreases strongly and reducing the advantage of grid-less front surface.

5.2.7 Towards high-efficiency

Currently the highest IBC-BHJ cell efficiency of 25.6% has been demonstrated by Panasonic [344]. This result overcomes the 25% efficiency barrier in place for many years in a lab device obtained through photolithography steps [366]. It is interesting to note that this record has been obtained on very large area device (143.7cm²), and therefore is closer to production line than laboratory scale. Moreover this result demonstrated that the IBC-BHJ concept is among the most promising approach to achieve the highest efficiency on c-Si based solar cell. Since the record cell shows $V_{oc}$ a bit lower than the maximum reached on HIT cell [325], there is room to further improve the IBC-BHJ cell.

Record efficiency higher than 25% can be achieved if the cell fill factor will reach a value of 83%, as obtainable reducing the cell pitch and the contact resistance between metal electrodes and a-Si:H layers. But if the IBC-BHJ cell achieves fill factor values lower than 83% then the cell $V_{oc}$ must be enhanced to compensate for the lower fill factor. Even though
Voc value as high as 750 mV has been recently demonstrated by Sanyo-Panasonic on conventional transverse heterojunction cell, the same Voc seems not easy to achieve due to difficulties in performing a surface passivation of the gap between the two contacts able to nullify the SRV.

5.3 Future direction

The way to reduce the Si based solar cell cost and then the PV market price is represented by thickness reduction of Si wafer down to 100μm. On this thin wafer, low thermal budget technologies should be applicable to avoid wafer warping due to thermal stress. Si heterojunction device represents a valid choice as already demonstrated by Sanyo-Panasonic even on thin wafer [367]. Nevertheless Si heterojunction technology has three important unresolved issues. The first is the use of ITO, which is not available for very large cell production due to the presence of rare indium. The second is the Ag screen-printed pastes for the electrodes; indeed Ag cost has not been reducing as the rest of the cell, and accounts for about 30% of the total cell cost [368]. The third is the connection between cells within the module now ensured by conductive tape that introduced large series resistance. IBC-BHJ cell represents a potential solution for these issues. ITO can be potentially successfully replaced by ZnO:Al since the lateral conductivity is not an issue due to subsequent metallization. In order to reduce the cell cost, the Ag screen-printed contacts must be replaced by Cu plating. With respect to conventional solar cells, in which the front side grid shrinks to dimensions lower than 80μm to reduce the shadowing effect and material cost, the IBC device has lower geometrical constraints. Therefore the use of metal plating, in principle, should be easier to manage. But the adhesion of plated Cu still represents an issue that can be overcome by interlayer insertion such as nickel (Ni) or tin (Sn). Moreover the large amount of chemicals waste produced by the metal plating baths still represents environmental and cost concerns for the industry. To overcome this problem an innovative solution has been recently proposed
in Ref. [369]. It is based on locally plating by dynamic liquid meniscus formation, as depicted in Fig. 50. With the aid of this meniscus all the wet chemical technologies can be performed, such as local plating, etching and deposition from liquid phase. Since the liquid meniscus is only locally in touch with the wafer, it can be used to deposit Cu or other metals only where there is a specific necessity, thus strongly reducing the waste chemicals produced by conventional light induced plating systems [370]. With the aid of this new approach the metal contact of the IBC-BHJ may potentially not represent an issue [369]. The problem related to low fill factor of PV module due to the cell interconnection, conventionally made by conductive tape between the heterojunction within the module, can be easily overcome in IBC cell.

Fig. 50 Schematic diagram of dynamic liquid meniscus formation in touch with the substrate. From the pictures it is evident that the red fluid flowing from the center inlet is recalled back through suction at the left and right outlet. Therefore the fluid in contact with the substrate is always refreshed. With the aid of this meniscus all the wet chemical technologies can be performed, such as local plating, etching and deposition from liquid phase. Since the liquid meniscus is only locally in touch with the substrate, it can be used to deposit Cu or other metals only where there is a specific necessity, thus strongly reduce the waste chemicals always produced by conventional light induced plating systems. With this new approach, an issue related to low fill factor of PV module can easily be solved.

The design of module can be completely rewritten taking into account that both contacts are now on the same side of the cell. Therefore the IBC cells can potentially be done on a low-cost printed circuit board, instead of a conventional mylar sheet, where two interdigitated comb shape metal strips can ensure larger contact area between cells and
interconnections with respect to conventional ribbons. This can enhance the cell fill factor and the overall module efficiency.

### 6.0 III-V multi-junction on c-Si

Significant effort has been undertaken till date to reduce the cost of multi-junction solar cell (MJSC) technology by developing methods to manufacture them on low-cost wafers. The integration of III-V semiconductors on c-Si aims to improve efficiency and to solve the limitations encountered with other wafers such as germanium (Ge) or gallium arsenide (GaAs).

This review section focuses on the most relevant work done in the last years on the integration of III-V semiconductors on c-Si for the manufacture of multi-junction solar cells. Current state-of-the-art of the two most important techniques (epitaxial growth and wafer bonding) used for such integration are discussed. In addition to highlighting the most novel results obtained with each technology, current challenges and possible strategies to overcome them are also pointed out.

### 6.1 Introduction

MJSCs have demonstrated significant potential to reduce the cost and increase solar cell efficiency. Concentrator PV systems based on multi-junction solar cells boosts electricity generation and are expected to reduce the cost of PV.

The first key for the success of this technology lies in the ability to make affordable PV cells with very high-efficiency. Using concentration, the maximum conversion efficiency that can be achieved by a PV device with a single p-n junction on c-Si is 44% [371] for cells made from a material with an optimal bandgap ($E_g \sim 1.3$ eV). MJSCs are formed by stacks of several p-n junctions connected in series, each of which is intended to transform a portion of the solar spectrum into electrical energy with minimum losses. The ultimate efficiency of
MJSC with an infinite number of junctions is 86% [371], almost twice of that of cells with a single-junction. The second key factor for its success lies in the existence of a family of materials, namely III-V semiconductors, with excellent PV properties and ranges of suitable bandgaps to implement MJSCs.

The integration of III-V semiconductors on Ge has been successfully investigated in the last two decades. A MJSC on Ge has recently beaten the efficiency record for any PV device, achieving efficiency close to 42% [372]. However, the exploration of alternative wafers to Ge continues because of the shortage and relatively high costs of Ge.

Figure 51 Abundance of some elements in the Earth’s crust versus atomic number. The graph evidences the abundance difference existing between the Si and Ge (highlighted in red) in the Earth’s crust. Si is more abundant than Ge by a factor of $2 \times 10^5$. This difference turns into a big discrepancy in terms of the material cost and thus, the selection of Si as an alternative to Ge is clearly justified. Also, semiconductor devices are fabricated using Si, a unique electronic and PV material. An ideal candidate for multi-junction solar cells is Si. Data taken from [373], David R. Lide, ed., CRC Handbook of Chemistry and Physics, 85th Ed., CRC Press, Boca Raton, Fla., Taylor & Francis Group, 2005.

Figure 51 represents a plot of the abundance of some elements [373] in the Earth’s crust versus their atomic number. This plot shows that Si is a factor of $\sim 2 \times 10^5$ times more abundant than Ge in the Earth’s crust. Accordingly, the ideal candidate on which to manufacture multi-junction solar cells is c-Si (Fig. 51), the ubiquitous electronic and PV
material. Indeed about 95% of semiconductor devices are presently fabricated using c-Si [374].

According to the iso-efficiency contour maps for concentrated light depicted by Wanlass et al. [375] for a double-junction solar cell, theoretical efficiencies between 34 and 40% can be achieved with a c-Si bottom cell if an appropriate material with bandgap ranging from 1.34eV to 1.84eV is used for the top cell. Figure 52 makes evident that there is a wide variety of III-V materials that meet this requirement. Hence the challenge is to develop strategies to grow them with good PV quality on a c-Si wafer, which in turn has to be processed to obtain an equally good performing bottom cell.

Fig. 52 Theoretical efficiency of double-junction solar cells grown on c-Si wafer as a function of top cell bandgap. For top cell, an appropriate material is required with bandgap ranging between 1.34 and 1.84eV. According to this graph, the maximum theoretical efficiency can be obtained for III-V/c-Si double-junction solar cell by using gallium arsenide phosphide (GaAsP) as top cell with arsenic content of 0.8%. This GaAsP/c-Si couple has an excellent bandgap combination for maximum utilization solar spectrum. Data from [375],
6.2 Challenges and difficulties

The integration of III-V semiconductors on c-Si has been a long-sought desire by the microelectronic industry [374,376]. In the PV field, the integration of III-V compounds on c-Si was intensively investigated in the 1990s, achieving good results [377-379]. Here, it is worth mentioning the works reported by Fitzgerald’s group at the Massachusetts Institute of Technology, U.S.A., Umemo’s group at the Nagoya Institute of Technology, Japan. All these groups demonstrated the production of solar cells with efficiencies above 20% by following a variety of approaches. Despite the excellent results published for an AlGaAs/c-Si solar cell with a $V_{oc}$ of 1.57 eV, $J_{sc}$ of 23.6mA/cm$^2$ and efficiency up to 20% [380], the technology was not transferred to industry, possibly due to reproducibility issues or complexity in the process.

In spite of these excellent results, the intensity of research declined considerably during the late 1990’s due to the difficulties in improving material quality, and the rapid progress of Ge based MJSC technology. The above groups pointed out that the main challenges for III-V heteroepitaxy on c-Si are: (i) lattice mismatch, (ii) mismatch in thermal parameters, and (iii) defect confinement. In the following sub-sections, we review each of these challenges in detail.

6.2.1 Lattice mismatch

The obvious problem for III-V heteroepitaxy on c-Si has been the lattice mismatch between epilayer and wafer (Fig.53). For instance, the lattice constants of c-Si and GaAs—the two materials whose integration has been long sought, differ by around 4%.
Room temperature bandgap versus lattice constant of common elemental and binary compound semiconductors. Lattice mismatch is an issue between epilayer (III-V, e.g. GaAs) and c-Si wafer. This plot evidences the lattice mismatch between gallium arsenide (GaAs) and c-Si, and a small difference between gallium phosphide (GaP) and c-Si lattice constants. Lattice mismatch between GaAs and c-Si is around 4%. Epitaxial growth can accommodate lattice mismatched materials either by growing strained material or by growing material relaxed to its lattice constant. Multi-colored band in the figure is the energy range corresponding to visible spectrum.

Therefore, the development of strategies for epitaxial growth, which can accommodate this difference, has received special attention. These strategies consider either growing the material compressed/strained (i.e. pseudomorphic material) [381,382], or by growing the material relaxed to its natural lattice constant (i.e. metamorphic material) [383-387].

6.2.2 Mismatch in thermal parameters

One of the major problems for the growth of III-V materials on c-Si has been managing the different thermal properties of both materials [374]. Indeed, the problem of heteroepitaxy is not epitaxial growth itself, which is performed at high temperature, but the subsequent cooling of the samples. When samples are still at high temperature, their quality can be made excellent, despite the lattice mismatch. During the cool-down process, different thermal stresses in the sample generate dislocations, other crystalline defects or even cracks in extreme cases. To solve these issues, several efforts, such as lowering the growth temperature without losing quality in the samples, have been explored to develop epitaxial routines that produce lower thermal stress.
6.2.3 Defect confinement

Most crystalline defects, originating during the III-V/c-Si integration, occur at the hetero-interface. However, they can propagate vertically and eventually reach active layers of the solar cell, producing a degradation of its properties [374,388,389]. Therefore, the development of epitaxial growth procedures that favor the annihilation or the confinement of crystal defects in parts of the structure far from the active layers of the solar cell have been recently pursued.

6.3 Approaches for PV integration

Interest in the integration of III-V materials on c-Si has re-emerged lately in the PV research community [374, 386, 387, 390-394]. Currently, the most developed technique for such integration is the direct epitaxial growth of III-V compound on c-Si, due to reasonable scientific understanding of the processes involved in the heteroepitaxy. However, the search for alternatives has continued. In particular, wafer-bonding technique has received special attention by demonstrating promising results based on its ability to solve the limitations of epitaxial growth.

Here we review both techniques by describing their state-of-the-art, emphasizing the most novel results obtained with each technology, pointing out current challenges, and possible strategies to overcome them. Finally, the limiting factors and hurdles for efficiency improvements in each technology are also presented.

6.3.1 III-V on c-Si epitaxy

As we have mentioned before, the interest in III-V on c-Si integration, and particularly the III-V/c-Si epitaxy, has experienced a breakthrough over the last few years. The reasons for this are based on the progress in understanding the heteroepitaxy process of III-V semiconductors on c-Si [376]. Moreover, a new generation of metal organic vapor phase epitaxy (MOVPE) reactors has been developed, and metalorganic precursors adapted
for the growth at low-temperature are readily available. As mentioned above, the use of lower
growth temperature provides more opportunities to handle thermal stress associated with
heteroepitaxy. Finally, the adaptation of new techniques (i.e. strategies to overcome the
defect confinement) to c-Si wafers applied to the metamorphic growth of the InGaAs/Ge has
also contributed to this progress [395].

Despite the wide variety of III-V compounds (Fig. 53), only a few of them are suitable for
direct integration on c-Si wafers. On the one hand, the materials have to be selected in a way
that the bandgap combination (bottom and top cell) is optimum for harnessing the solar
spectrum. On the other hand, the lattice mismatch between both materials has to be
minimized for reducing the formation of structural defects. Unfortunately, only a very small
number of III-V compounds meet both requirements. Thus, two different approaches are
generally used for handling the epitaxial integration of III-V on c-Si: (i) the lattice
mismatched (or metamorphic), and (ii) the lattice matched approach.

(i) Lattice mismatched approach

A metamorphic material is the one that grows on a wafer with a different lattice
constant in a way that promotes its relaxation (i.e. its transition to its own lattice parameter)
mainly through the occurrence of misfit and threading dislocations at the interface.
Accordingly, the lattice mismatch approach consists of integrating two materials with a
different lattice constant, in a way that its accommodation is achieved by the generation of
structural defects at the heterointerface. If the propagation of threading dislocations is
minimized and the relaxation process is completed, then the resulting top surface has the
desired lattice constant and a good crystalline quality (this is known as virtual wafer).

Under this approach, III-V materials that can be integrated on c-Si are relatively are
larger, since lattice matching is no longer a requirement. Hence, III-V candidates are selected
to offer an optimum combination of bandgaps when integrating on a c-Si bottom cell. Two
compounds, viz. GaAs and GaAsP, are generally used for achieving high quality metamorphic III-V/c-Si double-junction solar cells (Fig. 52).

GaAs/c-Si: The integration of GaAs on c-Si wafer consists of direct growth (monolithic) of the III-V material on the wafer [374, 396]. The bandgap of the GaAS makes it very attractive for top cell (middle cell) in double-junction solar cell (triple-junction solar cell), as depicted in Fig. 52. However, as mentioned in Sec. 6.2, several problems exist for obtaining a defect-free and high quality GaAs/c-Si structure [397-400]. First, the growth of a polar on a non-polar semiconductor leads to the formation of a high density of antiphase domains (APDs) which should be controlled for a high quality structure. Work has been done for minimizing the formation and propagation of these defects [397,401]. Another problem found during the direct growth of GaAs on c-Si was related to the existing difference in their lattice parameter (Fig. 53). This difference promotes the generation of misfit dislocations at the GaAs/c-Si interface and threading dislocations, which can potentially propagate through the whole structure, and degrade the quality of the solar cell. Finally, the difference in thermal expansion co-efficients will not only favor the formation of dislocations, but also will promote the appearance of cracks during the cool down phase in the GaAs layer [397].

Different approaches intended to seal off these limitations have been used [398-400, 402-404]. As an example, the use of III-V intermediate layers based on compositionally graded buffers, together with thermal cycle annealing [398-400], and the use of lower temperature for the first few nanometers of the growth [399,402] were implemented for decreasing the dislocation density. The use of these techniques has brought the dislocation density from $10^9$-$10^{10}$cm$^{-2}$, for direct GaAs on c-Si, down to $10^7$cm$^{-2}$, which is equivalent to 1-4 ns in terms of minority-carrier lifetime in n-GaAs [405]. However, to produce high-efficiency III-V top cells, these lifetime values are still low [403,404]. In fact, a low $V_{oc}$ of
~900mV under AM0 conditions for single-junction GaAs cells on inactive c-Si wafers was measured in those cells [391].

The above mentioned incompatibilities make it very difficult to achieve a high quality GaAs/c-Si monolithic device. Hence, another alternative was considered for such integration. This approach consists of modifying the lattice constant of the c-Si wafer through the use of group-IV buffer layers. The most developed method so far is the use of a Ge\textsubscript{x}Si\textsubscript{1-x}/c-Si virtual wafer [386,391,406-408]. The SiGe is an intermediate layer aimed to modify the Si lattice constant by increasing the Ge content during the epitaxial growth. Therefore, the lattice constant can be increased from 5.43Å (Si) to 5.64Å (Ge), and provide a new template with a lattice constant closer to the one of GaAs (5.65 Å). However, during the relaxation process, some misfit dislocations are generated. Some of them can eventually fold up and turn into threading dislocations, which degrade the device performance [406].

Despite the limitations of this technique, promising results were obtained for GaAs solar cells grown on SiGe/Ge wafers. Recently, dislocation densities as low as 8x10\textsuperscript{5}cm\textsuperscript{-2} within the relaxed GaAs layer were obtained using Si/Ge wafers for III-V/c-Si integration. This value corresponds to a minority-carrier lifetime of 10ns for n-type GaAs. To the authors’ knowledge, this is the highest value reported so far for GaAs grown on c-Si [409], resulting in efficiencies higher than 18% for single-junction GaAs solar cells on c-Si wafers [383,409].

Promising results have been reported recently on MJSCs based on SiGe wafers [386,391,406-408]. High quality indium gallium phosphide (InGaP)/GaAs double-junction solar cells have been successfully grown on c-Si wafer through the use of Ge virtual wafers with SiGe step-graded buffers [386] achieving \textit{V}_{oc} of 2.2V and an efficiency of 15.3 % for AM0 conditions [386, 410]. A InGaP/GaAs/SiGe triple-junction solar cell with an efficiency of 20% under AM0 (1 sun) illumination, and an open circuit voltage higher than 2.6V has been recently reported [411]. Wang et al. [412] have recently reported a GaAsP/SiGe double-
junction solar cell with an improved bottom cell structure, within a current matching scenario, with efficiencies up to 20.6% using 1 sun illumination. This work proposes the use of light trapping techniques and a further optimization of the bottom cell for maximizing the device performance.

GaAsP/c-Si solar cell: As it has been described before, in the metamorphic approach, materials are selected to offer an optimum combination of bandgaps. In this respect, the maximum theoretical efficiency of 40% has been obtained for a III-V/c-Si double-junction solar cell with top cell material bandgap of 1.66 eV (Fig. 52). This ideal material can be obtained by adding arsenic to GaP to produce GaAs$_{1-x}$P$_x$ (or simply GaAsP). In particular, the optimum composition (see Fig. 52) is a GaAsP alloy with 80% arsenic and 20% phosphorus in the group-V sublattice (i.e. GaAs$_{0.8}$P$_{0.2}$).

Due to the mismatch between top and bottom cell materials, the integration of GaAsP on c-Si is performed through the creation of a virtual wafer, which takes care of the lattice constant transition and the defect confinement [413, 414]. Therefore, the resulting top surface has the desired lattice constant and a good crystalline quality, in which the GaAsP top cell could be easily integrated.

The virtual wafer consists of an initial III-V layer lattice matched to c-Si to obtain a defect-free III-V template and addresses the problems related to the growth of a polar on a non-polar c-Si wafer [415-418]. The ideal material for this is GaP since it has a lattice constant reasonably close to that of Si (Fig. 53). After this step, the growth of a GaAsP graded buffer layer is included on top of the nucleation layer to handle the lattice parameter transition from Si to GaAsP and confinement of threading/misfit dislocations (Fig. 54).
Fig. 54 Schematic diagram for the metamorphic integration of gallium arsenide phosphide (GaAsP) on c-Si wafer. This process involves the growth of polar material (gallium phosphide GaP) on non-polar wafer (c-Si) which results in poor morphological quality (i.e. non-homogeneous nucleation layer/isolated islands). To ensure high morphological quality, layer-by-layer growth is required for the integration of GaP over c-Si. GaP acts as a virtual wafer. The integration of GaAsP over c-Si is performed through the virtual wafer. The virtual wafer takes care of lattice constant transition (from Si to GaAsP). Therefore, GaP is grown over c-Si since GaP has a lattice constant close to Si. GaAsP graded buffer is grown on top of a GaP nucleation layer for accommodating the lattice mismatch between the top and the bottom subcell materials (i.e. p+-c-Si and GaAsP).

While GaP has been reported to be the most ideal candidate for the nucleation layer, the growth of GaP on c-Si presents some limitations, mainly due to the growth of a polar (GaP) on a non-polar c-Si wafer [415-418]. In fact, the growth of a polar on a non-polar wafer has been reported to favor a non-homogeneous nucleation layer, formed by isolated islands, typical from a three-dimensional (3D) growth [419-421]. Moreover, the important thermal expansion coefficient mismatch [417] (the one for GaP is 2.3 times larger than that of Si) hinders this integration. In general, a layer-by-layer growth is pursued for the integration of GaP on c-Si wafers to guarantee a high morphological quality of the nucleation layer. Moreover, wafers must be properly treated before nucleation (i.e. single domain structure formed by double steps in the absence of silicon oxide) for minimizing the appearance of planar defects, which otherwise, might ruin the electrical behavior of the solar cell; and for obtaining a defect-free template for the integration of the GaAsP graded buffer.

Inspite of the significant amount of effort that has been done to find the best conditions for obtaining a continuous, defect-free GaP surface, this topic remains an open issue. The beneficial effect of low-temperature nucleation on obtaining a high quality and
defect-free surface has been reported [422, 423]. On the other hand, Ref. [388, 424] support the idea of using high nucleation temperatures, together with very high V/III ratios to obtain a smooth and APD-free structure [388, 424]. In any of those cases, a defect-free GaP layer has been successfully grown on vicinal <100> c-Si wafers. The resulting GaP/c-Si virtual wafers serve as templates for further III-V integration.

Going from GaP to GaAsP involves a significant increase in the lattice constant that, if not addressed properly, will produce a high concentration of dislocations and crystal defects that will ruin the PV performance [384, 387]. In this case, a metamorphic GaAsP buffer layer, with variable arsenic content, is grown on the GaP nucleation layer (Fig. 54). The purpose of the buffer layer is to make an optimal transition between the nucleation layer and the layer with the composition needed for the top subcell (ideally GaAs$_{0.8}$P$_{0.2}$, in this case). This layer will absorb/avoid the propagation or will even annihilate crystal defects that will be generated when the gradual change of the lattice constant (i.e. the composition) occurs during growth. In other words, the goal of the buffer layer is to create a III-V virtual wafer of high crystalline quality with a different lattice constant than that of the Si that supports it. Eventually, this virtual wafer will serve as template where GaAsP top cells of the adequate bandgap can be integrated, thus forming a GaAsP/c-Si double-junction solar cell (Fig. 55a) with a high theoretical efficiency (Fig. 52).

The development of metamorphic GaAsP/c-Si solar cells has received special attention over the years. Several research groups [377, 384, 385, 425, 426] have been working on the development of the structure depicted in Fig. 55a. Their efforts have been mostly directed towards the optimization of key steps in the epitaxial growth of III-V compounds on c-Si, such as nucleation layer, graded buffer, and top subcell. The main target has been the minimization and confinement of crystal defects in the structure. Consequently,
high structural quality graded buffers and promising results in the reduction of the dislocation
density and annihilation of APD have been reported [384, 388, 390].

Fig. 55 (a) Ideal GaAsP/c-Si (or GaInP/c-Si) double-junction solar cell structure based on the metamorphic
approach. The accommodation of the lattice mismatch is handled through the growth of a GaAsP graded buffer
layer. The simplification of this structure turns into a single-junction GaAsP solar cell grown on top of an
inactive c-Si wafer, as depicted in (b). When c-Si wafer acts as template (inactive wafer), technical challenges
associated between the formation of c-Si bottom subcell and the subsequent formation of the tunnel junction can
be avoided. Therefore, III-V subcell optimization can be done easily. Data for the latter from [427], Grassman T
J, Carlin J A, Ratcliff C, Chmielewski D J, Ringel S A., Epitaxially-grown metamorphic GaAsP/c-Si double-
junction solar cells, 39th IEEE PV Specialist Conf. (Florida) 2013, pp. 0149-0153.

However, there are still some key parts of the structure which have not received
enough attention in the past, and those optimization is crucial for obtaining high quality
double-junction solar cell.

The first key point is the formation of c-Si bottom subcell with an optimum emitter (in
terms of doping and thickness) and maintaining low roughness over the c-Si surface for
subsequent epitaxial growth. Although an important progress on the optimization of bottom
cell has been reported recently [428], most groups so far used c-Si wafer as a mere template
(i.e. inactive wafer) and did not work on bottom cell optimization [377,384,385,387,390].
This alternative (i.e. c-Si as inactive wafer) simply avoids the problems associated between
the formation of the c-Si bottom subcell and the subsequent growth of the tunnel junction since c-Si wafer only acts as mechanical support and crystallographic template for the structure. In this way, the optimization of the III-V subcell can proceed independently and a lateral conduction layer is often included in the III-V solar cell [427] to ease the formation of rear contact (Fig. 55b). Both top and bottom contacts are formed on III-V layers. Promising results on obtaining a high-efficiency single-junction GaAsP grown on an inactive wafer has been reported so far. Lang et al. presented n+/p-GaAsP/c-Si solar cell with $V_{oc}$ of 1.10V [385]. Furthermore, Grassman et al. [384] reported promising light I–V ($V_{oc} = 1.04V$, $J_{sc} = 13.1mA/cm^2$) and EQE results for a GaAsP/c-Si single-junction prototype solar cell. The idea is that these structures could be eventually integrated on optimized c-Si bottom subcells for obtaining high quality GaAsP/c-Si double-junction solar cell.

The second key point is the formation of a tunnel junction to electrically connect the bottom and the top cell. The aim is to introduce highly doped ($>10^{19}$/cm$^3$) layers of a GaAsP homostructure [429] or a GaInP/GaAsP heterostructure. Latter is preferred since it has been recently demonstrated that its use reduces optical losses [426]. Preliminary work has been performed in this area, and promising results were obtained for c-Si based MJSC [426]. However, still some work [429] has to be done to refine the structure and to reduce optical absorption of the tunnel junction.

Although a great deal of work has to be still done for achieving high quality III-V on c-Si double-junction solar cell, a prototype of a GaAsP/c-Si double-junction solar cell [425,427] has recently been reported. This structure has been epitaxially grown by combining the use of molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD) reactors. The success of this prototype lies in the use of an optimized (i.e. defect-free) GaP nucleation layer, which acts as a template for a high quality GaAsP metamorphic
graded buffer. Interesting results were obtained in this case, demonstrating the operation of a double-junction solar cell, with $V_{oc}$ of 1.62V and $J_{sc}$ of 11.0mA/cm$^2$ [425].

Though interesting results reported [425,427] for as-grown tunnel junction test structure (i.e. peak tunneling current densities of 3A/cm$^2$), its integration on the double-junction structure degrades its properties as a result of its exposure to high temperatures during the top cell growth. Thus, it limits the electrical behavior of the double-junction solar cell. Nevertheless, the obtained results are promising, demonstrating that the technology for such integration is progressing and that current technology is not very far from obtaining a high quality GaAsP/c-Si metamorphic double-junction solar cell.

(ii) Lattice matched approach

As discussed above, one of the main limitations of III-V on c-Si epitaxy is the mismatch in lattice parameters. Hence, it is straightforward to assume that a lower lattice mismatch between the wafer and III-V compound implies a better structural quality of the resulting structure. Despite the fact that GaP seems to be the ideal candidate for the top cell material due to its lattice constant proximity to that of c-Si (Fig. 53), its large bandgap (2.2 eV) makes it unsuitable for the top cell material. Therefore, a different material must be considered for the top cell. In this case, the most studied material for such integration is the quaternary alloy GaNPAs [381, 382, 430].

Here, the lattice mismatch between the bottom (c-Si) and the top cell (GaAsP) is reduced by introducing nitrogen into the III-V semiconductor that decreases its lattice constant and brings it closer to that of Si. The idea is to grow the direct bandgap III-V alloy Ga$_x$N$_{1-x}$P$_{1-y}$As$_y$ (hereafter GaNPAs) onto the c-Si wafer and minimize the formation of structural defects [381, 382, 430] for high-efficiency double-junction solar cell. In 2004, Geisz et al. first reported the lattice-matched GaNPAs on c-Si double-junction solar cell [381]. As depicted in Fig.56, the cell is formed by a n-on-p c-Si bottom subcell, a
GaP:Zn/GaNP:Se tunnel junction, and a GaNPAs (E_g ~1.8 eV) top subcell. As in the case of the metamorphic approach, to minimize the occurrence of crystalline defects [381, 382], a GaP nucleation layer is also grown before the GaNPAs layer.

The use of nitrides (even diluted nitrides) for reducing the lattice mismatch presents an important drawback: the formation of nitrogen-related defects, which greatly reduce the diffusion length in the GaNPAs layer, and limits the performance of the top junction [390]. Geisz et al. [381] proposed the use of a field-aided device through a p-i-n configuration in the top cell to maximize its IQE, and to avoid the limitations of the extremely short diffusion length measured in the top cell. Thus, a thick GaNPAs intrinsic layer was grown to enhance the performance of the device (see Fig. 56).

![Fig. 56 GaNPAs/c-Si lattice matched double-junction solar cell. To reduce the lattice mismatch between the top cell and bottom cell, nitrogen is introduced in the III-V structure to reduce its lattice constant and bring it close to that of Si. Also, nitrogen minimizes structural defects. In the bottom cell, BSF acts as reflector for minority carriers and causes the minority carriers (electrons in this case) to move to the bulk towards the p-n junction and reduces surface recombination at the rear side. The internal quantum efficiency has been maximized through the introduction of a field-aided device in the top cell (i.e. p-i-n configuration). In this double-junction structure, top cell limits the device current. Redrawn from [381], Geisz J F, Olson J M, Friedman, D J. Toward a monolithic lattice-matched III-V on c-Si double-junction solar cell, 19th European Photovoltaic Solar Energy Conference (Paris) 2004.](image)

Interesting results were obtained for each subcell measured separately [431]. For c-Si bottom cell, V_oc of 536mV and J_sc of 14.5mA/cm^2 have been reported. GaNPAs (E_g ~1.8eV)
top cell showed $V_{oc}$ of 1.09 V and $J_{sc}$ of 5.7 mA/cm$^2$. This double-junction structure has the potential for further improvement, since the top cell limits the device current ($V_{oc} = 1.53$V, $J_{sc} = 6.3$ mA/cm$^2$, AM1.5G efficiency = 5.2%). Currently, efforts are mainly focused on: (i) reducing the dislocation densities of the buffer layer through a better control of the GaP nucleation layer, (ii) forming a functioning tunnel junction by increasing the p-type doping, and (iii) increasing the top cell current by reducing the emitter sheet resistance and controlling the material quality of the GaNAsP top cell [431].

6.3.2 III-V on c-Si using bonding technique

Different alternatives for the epitaxial integration of III-V semiconductors on c-Si wafers have been reviewed so far. However, as described above, this technique presents some limitations, which include: (i) as described in Sec.6.3.1.2, monolithic integration is limited due to lattice matching requirements, which highly reduce the range of III-V materials that can be integrated on c-Si, (ii) the use of metamorphic growth techniques for integrating lattice-mismatched compounds is limited due to relatively high dislocation density formed in the buffer layer (Sec.6.3.1.1). In this regard, alternatives to this process have been recently explored. In particular, the mechanical stack has emerged as an alternative to avoid the limitations of the epitaxial process.

Unlike epitaxially grown structures, the wafer bonding interfaces are incoherent. This implies that it is possible to accommodate any lattice mismatched material without the formation of the above mentioned misfit dislocations [393,394]. Therefore, the use of wide variety of materials, including the ones discarded for conventional epitaxial growth, is allowed for this technique.

The physical concept of wafer bonding is based on the idea that two surfaces can stick together as long as the surfaces are perfectly polished, resulting in relatively very little friction between them [432]. In particular, in the wafer bonding technique, this consists on
transferring a thinned wafer of III-V compound (such as GaAs) to a c-Si wafer. The bonding can be carried out even at room temperature as a result of the interaction of pure surfaces by van der Waals forces. In order to guarantee a high quality bonding, surfaces have to be specularly polished and completely clean to avoid any organic contamination [433].

There are different wafer bonding approaches for the integration of III-V compounds on c-Si wafers for PV applications. One of them is based on high-temperature sticking of wafers. In this case, wafers are covered by a glass-like coating that bonds the wafers once the softening temperature is reached. However, this technique presents some limitations due to the use of high temperatures that may cause some problems such as defect generation, diffusion of impurities, thermal stress, etc. [434, 435].

An interesting alternative is the smart cut technology. The procedure for wafer bonding using this technique is depicted in Fig.57. Initially, handle (c-Si) and donor (GaAs) wafers are coated with a thin Si oxide, since the bonding of Si oxide surfaces can be done at room temperature in air. In some cases, a thin SiN layer is deposited before the oxide layer, in order to favor the adhesion of the III-V compound to the oxide (Fig. 57a). Then, a weakened layer (formed by hydrogen or helium bubbles) is generated within the donor wafer by the ion bombardment method (Fig. 57b) [392]. This layer will eventually serve as a predetermined breaking point. Next step is the preparation of the surfaces for lowering the surface roughness to obtain good wafer bonding. After putting them into close contact, both wafers are bonded together as a result of the oxide softening and the application of pressure (Fig. 57c). After wafer bonding, the exfoliation, i.e. detachment of GaAs wafer along the implanted layer, is achieved by a heat treatment (Fig. 57d). In order to avoid shearing of interfaces and separation of both connected materials, it is preferable to work with the lowest possible temperature, especially when materials with very different thermal expansion co-efficients are bonded. Several groups are exploring different ways for reducing the exfoliation.
temperature [394,436]. Finally, chemical and mechanical treatments of the exposed GaAs surface are required for obtaining high quality surface for subsequent epitaxial growth. In this technology, the donor wafer can be reused after exfoliation, and therefore the cost of the process is highly reduced (as compared to epitaxial growth on GaAs wafers).

Fig. 57 Illustration of the smart cut technology for GaAs/c-Si structures: (a) the process starts with two different wafers (i.e. GaAs as donor wafer and c-Si as handle wafer), both are oxidized to favor bonding. To improve adhesion between GaAs and Si oxide, in the donor wafer, a thin SiN layer is deposited before the oxide layer deposition. (b) a weakened layer is generated within the donor wafer by hydrogen ion implantation through the oxide, (c) two wafers are hydrophilically bonded together due to oxide softening and external pressure, (d) finally, after bonding, the GaAs wafer is cut away using the implanted region as a reference. Heat treatment is used to detach GaAs wafer. Chemical and mechanical treatment is required for the exposed GaAs surface for subsequent epitaxial growth. The remaining GaAs wafer can be reused afterward for subsequent processes.

The use of smart cut technology leads to good quality crystals with a low dislocation density below $4 \times 10^5 \text{cm}^{-2}$ [392]. Using smart cut technology, 12% efficiency GaAs/c-Si single-junction solar cells have been reported [392].

Other III-V materials such as indium phosphide (InP) have also been used as donor wafers for their direct bonding on c-Si wafers [437, 438]. These InP/c-Si stacks have been used as templates for subsequent III-V epitaxial growth, obtaining InGaAs/InP solar cells on inactive c-Si wafers [437] with $V_{oc}$ of 0.30 V, $J_{sc}$ of 24.9 mA/cm$^2$ and AM1.5G efficiency of 13.6%. This InGaAs solar cell is a good candidate for working as the bottom cell of a high-
efficiency triple-junction cell, since it may be current matched with InGaP/GaAs double-
junction solar cells [439, 440].

However, the use of this technique presents an important drawback: the bonding
layers are made of Si oxide, an insulating material. Thus, the c-Si wafer is not the active
region of the structure; on the contrary, it is merely acting as a mechanical support for the
structure without any active PV role. Hence, this technology requires the development of a
new solar cell design for contacting the rear side of the solar cell. With this aim, as shown in
Fig. 58, a lateral conduction layer [392] is grown on the top of the III-V seed layer (before
growing III-V solar cell epitaxially) for contacting the base layer of the active region.

Many groups have been working on solving the drawback of the inactive wafers [393,
441, 442]. As a result, an improvement of smart cut technique has been achieved. The main
modification is the substitution of the insulating bonding layer by a conductive layer. The
surface-activated wafer bonding process has been illustrated in Fig. 59 [442]. In this case, the
GaAs wafer is used as a template for epitaxial growth of III-V compounds (Fig. 59 a-c). An
etch-stop layer and a bonding layer are grown on top of GaAs wafer, before the epitaxial
growth (Fig. 59b). Simultaneously, as shown in Fig. 59 (d-f), the c-Si wafer is processed
before stacking, so a single-junction c-Si solar cell is formed. The whole structure is then
attached to a wax-type transfer substrate. Afterwards, the etch-stop layer is etched away
laterally, so the GaAs wafer is physically detached from the structure in a way that allows for
its reuse (Fig. 59c). In this process, the surfaces of the cell structures are cleaned by a beam
of argon (Ar) atoms in a ultra high vacuum chamber. The wafers are brought into intimate
contact immediately after the surface activation to initialize the bonding (Fig. 59g). Finally,
the wax-type transfer substrate is removed and the mechanical stacked solar cell is eventually
processed (Fig. 59h).

To our knowledge, the first direct wafer bonded MJSCs with a c-Si subcell was
reported on 2012 by Tanabe et al. [393], using an AlGaAs/c-Si double-junction solar cell,
with an efficiency of 25.2% under one sun (100mW/cm²) illumination. GaInP/GaAs/c-Si
triple-junction solar cell with an efficiency of 20.5% under one sun, and 23.6% under 71 suns
illumination (AM1.5 conditions) was also reported using the same technique [441, 442].
Recently, a GaInP/c-Si double-junction solar cell formed by a rear heterojunction GaInP and
a back junction, back contacted c-Si bottom cell has been reported [443] with an encouraging
efficiency of 26.2% at 1 sun illumination (AM1.5G).

Fig. 59 III-V/c-Si multi-junction solar cell by surface activated wafer bonding process: (a) GaAs wafer for
epitaxial growth of III-V compound, (b) etch-stop layer and bonding layer are grown right before the epitaxial
growth of III-V solar cell and then attached to a transfer substrate, (c) lateral etching remove etch-stop layer and
GaAs wafer is detached for reuse, (d-f) single-junction c-Si solar cell process, (g) after cleaning and activating the surfaces, wafers are bonded together, (h) wax-type transfer substrate is removed and stacked MJSC cell is processed for top contact. This process is an improvement of smart cut technique, supporting wafer (c-Si) is not inactive. Supporting wafer is active and used to form bottom cell.

Although promising results have been achieved recently, the main bottlenecks of this technology are the resistance of the bonding surface, and current mismatch between the subcells, which limits the device performance. This is primarily limited by the c-Si bottom cell [441]. For a better visual comparison of various technologies associated with III-V on c-Si MJSC, a block diagram is shown in Fig.60.

Fig. 60 Different III-V compounds on c-Si technology. The integration of III-V semiconductors on c-Si wafers by epitaxial growth using two different approaches: lattice matched and lattice mismatch (or metamorphic) approach. The main difference between these two approaches lies on handling the lattice mismatch between the top and the bottom cell materials. These two different approaches have been found to produce successful results for the integration of III-V on c-Si wafers through the wafer bonding approach. An important process is the surface activated process, which replaces the isolating bonding layer (used in the smart cut technology) by a conductive layer, and thus, the c-Si wafer takes place in the active region of the structure and acting as bottom cell.

6.4 Future outlook

Two different technologies have been predominantly used so far for the integration of III-V on c-Si: epitaxial growth, and wafer bonding. Epitaxial growth of III-V semiconductors
on c-Si wafers has received a lot of attention over the last decades, resulting in a reasonable scientific understanding of this process. Although a great deal of work has to be still done for achieving high quality monolithic III-V on c-Si double-junction solar cell, a prototype of a GaAsP/c-Si double-junction solar cell [425,427] has been recently reported. This structure has been epitaxially grown by combining two different techniques: MBE, and MOCVD. Interesting results were obtained in this case, demonstrating the operation of a double-junction solar cell, with $V_{oc}$ of 1.62 V and $J_{sc}$ of 11.0 mA/cm$^2$ [425]. These results are promising, and demonstrate that the technology for such integration is progressing. Future work will be directed towards the development of the tunnel junction and its integration into the double-junction solar cell, which is the main bottleneck for this structure, limiting the electrical behavior of the double-junction solar cell. Moreover, future activity must be directed towards simplification of the technology by means of the development of a GaAsP/c-Si metamorphic double-junction solar cell into a single reactor (i.e. MOCVD).

On the other hand, wafer bonding has emerged as an alternative for epitaxial growth. In particular, the surface-activated wafer bonding technology is seen as a promising option for III-V on c-Si integration. In this respect, a GaInP/c-Si double-junction solar cell formed by a rear heterojunction GaInP and a back junction back contacted c-Si bottom cell has been recently reported [443] with an encouraging efficiency of 26.2% at 1 sun illumination (AM1.5G). In this case work must be directed to overcome the current limitations, such as resistance of the bonding surface and current mismatch between cells, which are currently the limiting factors of the cell electrical properties.

7. Amorphous Si solar cells

A-Si:H has seen rapid development in industrial processing in the last decade, and has led to multiple types of large area and roll-to-roll deposition systems. While the Si material
development appears to have reached saturation, the passive parts of devices, such as surface
texture, light trapping designs, development of thinner cells, and cells on new exquisite
nanopillar and nanohole structures have made tremendous progress. Moreover, third
generation concepts are beginning to be applied to thin-films Si devices, making a paradigm
shift in the way a solar cell operates, with existing fabrication tools.

7.1 Introduction

According to European Photovoltaic Industry Association (EPIA) the global
cumulative installed solar power capacity in 2015 crossed 228GW [444]. The learning curves
[445] show a 22% reduction in price for PV; thin-film PV shows a slightly higher rate of cost
reduction compared to c-Si wafer type of cells. Though the cost of thin-film Si modules
commercially is less than that of c-Si, the cost of electricity is essentially similar in both
cases. This makes a c-Si module still most attractive because of its high-efficiency. Among
thin-film PVs, CdTe is the most attractive, due to a very small energy payback time of 0.5
years [446] at the cost of ~$0.6/W [447]. These advances clearly pose a commercial
challenge for a-Si:H PV.

The commercial single-junction a-Si:H modules have an efficiency of 4-8%, whereas
the best laboratory efficiencies are in the range of 9.5-10%. According to International
Renewable Energy Agency, among thin-film technologies, a-Si:H thin-film is perhaps the
most challenged by the current low-cost c-Si [448]. Its future is rather uncertain as some
producers have recently either stopped or reduced part of manufacturing capacity, even
though in laboratory it is demonstrated that using a simple thin a-Si:H absorber a stabilized
efficiency of 10% can be achieved [449,450]. Moreover, the energy payback time of thin-
film a-Si:H, as was claimed by TEL Solar Japan (formerly Oerlikon), is less than 1 year, and
a cost of electricity of $0.088/kWh for ground mounted system is estimated [451]. The
wholesale price of thin-film a-Si:H PV module in July 2013 is only $0.46/Wp and thin-film
a-Si:H/µc-Si:H (micromorph) is at $0.59/W_p$, much lower than $1.74/W_p$ in the beginning of 2010 [452].

According to EPIA fact sheet [453], the most critical materials used in PV technologies are indium, tellurium and Ag. The first two of these are indispensible elements of the state-of-the-art CIGS and CdTe solar cells respectively. However, these elements are not absolutely necessary for thin-film Si PV, especially for superstrate type of cells. Typical schematic diagram of a p-i-n (also called superstrate type) and an n-i-p (also called substrate type) a-Si:H cell is given in Fig.61. ITO is generally used on the top TCO for n-i-p cells, and Ag is used as rough template on which n-i-p cell is made. The former can be replaced by an alternative TCO, such as doped ZnO:Al [454], whereas many types of light trapping features at the back side can be made; patterning of the substrate (through lithography or embossing techniques) [455], naturally grown textured ZnO [454], and texture etched ZnO [456]. For p-i-n cells, white paints [457-459], white sheet (developed by Dupont for Oerlikon) [460], and Al [461] can be used as back reflector. However, Ag is still used by many companies to maintain a high-efficiency. A trade-off has to be made between gain in price for high-efficiency, and the loss due to high cost of Ag in comparison to Al. Since the price of Ag has fallen recently after a peak in 2011 of above $1100/kg to now (in 2016) around $500/kg [462], this may currently not be an issue with PV, but may be sensitive to future demand-and-supply. As efficiency increase is an option to reduce the cost [463] (every 1% increase in PV module efficiency reduces the balance of system (BOS) cost by between $0.07 and $0.10/W), micromorph cells are best suited to serve this purpose with relative simplicity and high-efficiency. Commercial micromorph module efficiencies are between 6.5 and 9%, though best laboratory efficiencies are currently in the range of 12-13%. It should be noted that prototype module efficiencies of up to 11% have been demonstrated. Further efficiency increase by employing higher number of junctions will have to take into account the possible
cost benefit of a high-efficiency and complexity of production. Bankruptcy of Unisolar Ovonics (US) after years of experience in triple-junction cells, and difficulty of other companies, especially Kaneka Co. (Japan), in commercializing such products warns us that careful design and process simplicity have to be developed for cost reduction, especially the capital expenditure (CAPEX), and a new industrially viable processing is a necessity.

In this section we will look at how the thin-film Si technology has evolved through the years and show that, in spite of current uncertainty in market, why it is still one of the most promising technology for the future.

7.2 Brief history and status of thin-film Si technology

A-Si:H came into existence in 1960s. Amorphous structure contains short range order similar to c-Si but deviates in medium range and long range order. The second difference is that critical (average) network coordination for a-Si is 2.4 compared to coordination of 4 for...
c-Si. Breaking of bonds allows the material to reduce the coordination. Hydrogen has a big role in reducing the network coordination while retaining local four-fold coordination. Hydrogen is situated at monohydrides, dihydrides, polyhydrides \((\text{Si-H}_2)^n\), \(\text{SiH}_3\) and voids. The material can be described as continuous random network which contains randomly distributed weak bonds and dangling bonds. However, the structure also contains another phase which is hydrogen rich, with low density regions and voids. It was in 1976 that an a-Si:H solar cell with 2% efficiency was made, with a prediction of 15% efficiency in the future \([464]\). However, it was realized that these materials (cells) suffer from light induced degradation, also called Staebler-Wronski effect, discovered in 1977 \([326]\). This phenomenon, with a decrease by an order of magnitude in both dark and light photoconductivity under illumination from the initial state, is metastable. All optoelectronic characteristics can be reverted back to the initial state by annealing of the sample above 150°C (above the glass transition temperature of hydrogen in amorphous material). This phenomenon is caused by a change in midgap density of states (increase in dangling bond density) resulting in shift of Fermi level towards midgap and increase in recombination. There are basically two divergent models proposed as origin of this effect; (i) (weak) bond breaking (hydrogen mediated) that creates isolated defects \([465-467]\), and (ii) voids/volume deficiencies \([468-470]\). Hydrogen seems to play an important role in this effect. To mitigate the Staebler-Wronski effect, materials have been fabricated with low hydrogen content, smaller \(\text{Si-H}_2/\text{Si-H}\) ratio, lower microstructure factor/void content, lower Urbach energy (weak-bond density), etc. To that end, high hydrogen dilution of precursor \((\text{SiH}_4)\) gas during deposition is invariably used. Now, use of thinner absorber layers and multi-junctions cell design has made it possible to control the light induced degradation of efficiency to an acceptable range below 10%.
Fig. 62 Schematic diagram of typical micromorph superstrate type double-junction cells. An efficient tunnel recombination junction made of p- and n-µc layers allows Ohmic contact between the cells. ARC, normally a graded refractive-index layer (n) coating reduces partly the 4% reflection loss at the glass/air interface. Refractive index matching layer such as TiO2 has the function to reduce reflection at the TCO (n~2)/p-layer (n~4) interface; intermediate reflector selectively reflects light at the tunnel recombination junction to the top cell, a technique by which the top cell thickness can be substantially reduced for better stability. Typical intermediate reflector is made from oxides - SiOx (n or p-type) or ZnO or a Bragg reflector. Typical thickness and bandgap of the top cell and the bottom cell are ~200nm, 1.8eV and 1-2µm, 1.1eV respectively.

Later, alloying a-Si:H with C, Ge, N, O, etc. allowed fabrication of multi-junction solar cells with wide bandgap doped layers, and tunnel recombination junction. This was considered a major advantage as compared to c-Si cells. Up to beginning of 1990s, a-Si:H cells in combination with an a-SiGe:H alloy cells in multi-junction structure were considered as among the best options, and a number of industries focused on this technology (Solarex [471], Unisolar [472], Sanyo[473] and Fuji electric [474]). By 1990, double and triple-junction devices using a-SiGe:H as bottom cell(s) reached global AM1.5 initial efficiency of 13.0% and 13.7%, respectively. Throughout this period, however, a-Si:H PV went through a technological challenge because of “degrading cells” (the Staebler-Wronski effect of a-Si:H [326]), and even a-SiGe:H alloys showed substantial degradation [475]. However, the advent of device-quality nanocrystalline Si (nc-Si:H) absorber layer in mid 1990s, [476,477] and demonstration by Kaneka with cell efficiency of >10% at a high deposition rate (0.5nm/s) [478] changed the scenario. Thus, a-Si:H in combination with nc-Si:H (also called µc-Si:H) became desirable. This structure, called micromorph cell (Fig.62), allowed a greater range of solar spectrum to be absorbed, avoided the toxic and expensive germane gas, and demonstrated enhanced stability. This nc-Si:H material has attracted immense research
interest because of its complex structure and yet to be fully understood growth process [479].

A debate exists on whether a-SiGe:H or nc-Si:H is a more profitable proposition as the bottom cell [480]. The arguments are based on two different scenarios, i.e. whether to use expensive germane gas, lower deposition rate (~0.1nm/sec), but relatively thinner (~100 nm) absorber layer for a-SiGe:H, or a much thicker layer (>2µm), accompanied with degradation of cell performance at high deposition rates for nc-Si:H [481]. One of the strong arguments used for thin-film Si solar cells has been the non-toxic nature of base materials compared to other types of thin-films PVs. Germane gas is highly toxic, due to which the preference in the last decade has tilted in favor of nc-Si:H. Thin-film Si processing also uses toxic dopant gases (PH3, B2H6 etc.), however, their concentrations are very small in the gas mixture.

At present the most widely used industrial process is the micromorph structure. TEL Solar has provided even turnkey solutions for these double-junction cells. Though the use of a-SiGe:H in a double-junction structure is now rare, because a-Si:H/nc-Si:H potentially delivers higher efficiency due to perfect bandgap combination of 1.8 eV/1.1eV [482], a-SiGe:H still holds a lot of promise in triple-junctions, especially for the adjustable bandgap middle cell. The cell with current record initial efficiency of 16.3% (initial) uses a-SiGe:H in the middle cell [483] in an n-i-p cell configuration. Though the record stabilized efficiency is achieved without Ge in a p-i-n type a-Si:H (Eg ~1.73eV)/nc-Si:H (Eg ~1.1eV)/nc-Si:H (Eg ~1.1eV) structure [484,485], LG is exploring to use a-SiGe:H films to improve this technology [486]. LG developed a-SiGe:H cell with a modified E-shape bandgap profile, originally demonstrated at Utrecht University [487,488], which was used as the middle cell of a triple-junction structure and delivered an initial efficiency of 14.9%. Moreover, the direction towards thinner cells (to be discussed shortly) can only be achieved by using a-SiGe:H, even for double-junction cells. Moreover, it has already been demonstrated that a very stable a-SiGe:H can be made with protocrystalline (pc-Si:H) condition [489] (i.e. films
deposited just before the onset of microcrystalline regime known as protocrystalline condition), though at a low deposition rate (~0.06nm/sec). The success will depend on the fabrication of stable low bandgap a-SiGe:H (E_g ~1.3-1.4 eV) cell, especially at acceptable deposition rates (> 0.1nm/s). In this aspect, two types of development have taken place:

(i) μc-SiGe:H [490], which allows a use of a thinner bottom cell of a double (a-Si:H/μc-Si$_{0.83}$Ge$_{0.17}$:H [491]), and triple-junction (p-i-n type a-Si:H/μc-Si:H /μc-Si$_{0.9}$Ge$_{0.1}$:H [492], p-i-n type a-Si:H/μc-Si$_{0.6}$Ge$_{0.4}$:H/μc-Si$_{0.91}$Ge$_{0.09}$:H [493]). The total thickness of the double-junction [491] and the triple-junction [493] are only 1000nm and 1800nm, respectively.

(ii) HWCVD a-SiGe:H has [494] shown that good photosensitive materials can be made for bandgap even below 1.4eV, much better than PECVD grown materials. However, this process demands high gas flow rate to avoid depletion of the germane gas. The cost implication of high germane consumption has to be considered. Table 2 shows the record efficiencies of single, double, and triple-junction Si thin-film cells.

Table 2 Record thin-film Si cells. The bandgap and thickness of the layers are: a-Si:H (1.7-1.9 eV, ~200 nm), a-SiGe:H (~1.5eV, ~150 nm) and nc-Si:H (1.1eV, ~2000 nm). A-Si:H layers are deposited in protocrystalline condition. Whereas the stabilized efficiency of single-junction (even initial efficiency) is well below the S-Q limit of 29%, the maximum stabilized efficiency (13.44%) is still much below the theoretically estimated triple-junction of ~48%. The results suggest enough room for improvement in the cell performance for thin-film Si. *independently measured.
### 7.3 Challenges to a-Si:H technology

As compared to c-Si technology (which dominates around 87% of the market), thin-film PV has a relatively small share of 13% in the PV market. This is further dominated by CdTe, leaving behind only a very small market for thin-film Si. The main argument against c-Si PV is its high cost due to, among others, the use of thick absorber material compared to a-Si. However, this argument is now challenged. First, high price of c-Si in 2006, due to Si ingot price increase from $200/kg to $400/kg between 2007 and 2008 [504], led to a 30% reduction of Si material in the manufacturing process. Using thinner wafers (180-200µm now from earlier ~300µm), process automation and waste recycling, the Si use has now reached a low 5-10g/Wp [448]. The target is to reach the level of 3 g/Wp or less between 2030 and 2050, pushing the limit further. Moreover, Panasonic showed their best efficiency of 24.7% for HIT solar cell for a wafer thinner than 100 µm [505], and even 70µm flexible cells can be made. Attempts are now being made to push it further down to less than 50µm, though sawing and yield require further technological advancement. Moreover, thin-film c-Si by lift-off methods are also in progress [506], and 16.8% efficiency for 18 µm c-Si has been reported and cells even with 10µm (8.7%) have been made. Second, the price of polysilicon has dropped sharply and reached $20/kg in 2011 [504]. Third, the large production of c-Si based modules has reduced the price [445]. Moreover, the large over capacity has forced dumping of PV at low price (around 25GW of global installation compared to around 60GW of ramped module capacity in 2011) due to which even c-Si modules can be purchased at very low price and pushed thin-films PV to margin.
Among thin-film PV technology, CdTe made up 46% of total module production in 2012, followed by thin-film Si (a-Si:H single and multi-junctions, 35%) and CIGS (19%). However, CdTe production is dominated by only one company (First Solar) and CIGS is predominantly by Solar Frontier, clearly showing that these productions are still very much process specific. Wide use of off-the-shelf deposition facilities has still not taken place, unlike with thin-films Si, for which even turnkey solutions are available. Si, though, is expected to maintain its advantage over other thin-film materials, since it is non-toxic and abundant.

7.4 Deposition related issues

A-Si:H is grown from gas phase in a vacuum chamber. It is a very reproducible material, and is very weakly dependent on process parameters, deposition systems, reactor volume or pumping speeds, etc. Standard a-Si:H films are routinely made at many labs with various deposition processes, such as standard radio frequency (RF) PECVD, VHF PECVD, hot-wire CVD, microwave PECVD, PhotoCVD, etc., with deposition rates of 0.1-0.3nm/s with almost comparable physical characteristics, delivering around 10% initial efficiency in single-junction cells. However, for better stabilized efficiency, the deposition process is adapted. The first indication for a better stability against light soaking came with the hot-wire CVD a-Si:H [507] with a smaller hydrogen content (~1%) than that is in standard device-quality a-Si:H of 10%. Since then, it is more or less established that a-Si:H deposited under high atomic hydrogen ambient, which is generally, but not necessarily, made with high hydrogen dilution of SiH₄, just at the edge of transition to nanocrystalline regime is the most stable material. The amount of dilution H₂/SiH₄ depends on other deposition conditions; for example, LG uses a very high H₂/SiH₄ value of 60 for their a-Si:H top cell [501]. This material, called pc-Si (as mentioned already in Sec. 7.2) [508] is, however, sensitive to deposition process and is fabricated in a narrow deposition regime. Hence, it is prone to
irreproducibility and therefore needs good control in deposition process. Unlike a-Si:H, a pc-Si:H is thickness dependent. Hence it can make a transition to nc-Si:H with slight change in thickness. A competing process to make stable materials, and claims to be thickness independent, is the so called polymorphous Si (pm-Si:H) [509]. So far the stabilized efficiency with pm-Si:H has still not reached its full potential, and is yet to reach the efficiency that is obtained by pc-Si:H. One common denominator in all these materials is that they contain crystalline nanoparticles, brought in the material either by nucleation in the amorphous matrix (as in case of pc-Si:H), or embedded from gas phase (as in case of pm-Si:H). The correlation of stability with nanocrystalline incorporation, irrespective of its origin (whether through hydrogen dilution or Ar dilution of SiH₄) has been speculated for a long time [510].

Nc-Si:H can be made by a variety of techniques [511], the same that are used for a-Si:H. Control of ion energy with very VHF RF power and high process pressure have led to high quality nc-Si:H material, and cells with high-efficiencies above 10%. On the other hand, high RF power and high gas flows in high pressure gas depletion condition (also called HPD) has led to high growth rates. However, the monotonic decrease in material quality and solar cell performance at higher deposition rates [479] is still a lingering issue that needs solution.

7.5 Recent trends to push the limits: Light management

Light trapping in the absorber (intrinsic) layer is one of the most widely used concepts in thin-film Si solar cells for the purpose of either to increase the current or decrease the thickness of the absorber layer. This is essentially achieved in three ways [512]: (i) scattering: a random texture is generally used, (ii) geometric optics: features larger than the wavelength of light is used, the total internal reflections at interfaces of absorber layer is used for this purpose leading to $4n^2$ light passes in Yablonovitch limit [513], and (iii) diffraction: periodic pattern. The periodic designed pattern is brought about by hot embossing or nanoimprint
technology [455,514], photolithography plus etching [515], and direct patterning of the hard
substrate, such as glass [499]. The highest cell performance is still dominated by substrates
with random textures. A very recent study indicates that for thick cells with thickness in the
range of or higher than the wavelength of light, also called as geometric thickness, the
random structures will provide excellent light trapping effect. However, for thicknesses much
smaller than wavelength of light, a designed structure is needed to obtain higher current than
the random structure [516].

There are a number of techniques to manipulate the light behavior in a solar cell using
the light interaction at the interfaces of materials of dissimilar refractive indices. The novelty
here is to gain absorption without developing macroscopic textures that have adverse effect
on the growth of the absorber material, and lead to micro/macro defect states. Moreover, very
thin absorber layers can be used without the fear of shunting. Plasmonic effect of light
interaction at the interface of a metal (negative refractive index) and dielectric material
(positive refractive index) is exploited by embedded metallic nanoparticles/structures in a
solar cell [517]. The near field effect of increased absorption and the plasmon polariton
propagation of waves perpendicular to the length of the cells, bring down the necessary
thickness for the cell, whereas the scattering from the plasmonic structures additionally
benefit even thicker cells.

One of the positive outcomes of the research on designed substrate texture
architecture has been the development of almost any design and fine structure on any type of
substrate [518]. This has allowed for the fabrication of high-efficiency solar cells on
temperature sensitive substrates, such as cheap plastics PET, PEN [519], PC [520] etc. These
have temperature limitations due to their glass transition temperatures being less than 150°C,
which is much lower than the optimum deposition temperature (~200°C) of amorphous, or
c-Si:H material.
7.6 Current trend

Notwithstanding all the developments that have taken place for a-Si:H cells (see Sec. 7.2), efficiency is still an issue. The best stabilized efficiency for a triple-junction is still much lower than the best that CdTe (21% First Solar [521]) or CIGS (21.7% ZSW [522]) cells can deliver. Even with significant efforts, the defect density for a-Si:H and nc-Si:H intrinsic layers are still in $10^{15}/\text{cm}^3$ range, and a-SiGe:H has even more than an order higher defects. Moreover, light induced degradation issue of amorphous materials still persists. In the last few years, there has been limited research in the material side, and efforts have been directed towards the passive parts of the cells structure, mostly the optical design and light trapping. It has now been realized that with the best design used so far (solar cell on textured surface), the efficiency cannot be increased much further [523]; nc-Si:H growth limits the maximum root mean square roughness and opening angle of the surface feature that can be used, whereas the defect density limits the thickness of the a-Si:H and a-SiGe:H layers. Hence, new unconventional designs are being developed, of which two extreme cases are presented below; solar cells on (i) high aspect ratio structures, and (ii) flat surface.

7.6.1 Extremely thin cells

Traditionally, light trapping schemes, such as that described in the above section, are employed to mitigate the adverse effect of lower quality of a-Si:H layers compared to crystalline counterpart that compels the allowed thickness of the a-Si:H or nc-Si:H solar cells to be much smaller than the penetration depth of visible light. Industries, as well as research laboratories, are aiming for better stabilized efficiencies that are achieved with thinner cells. TEL Solar clearly identified this strategy as they brought out ThinFab and popularized the concept of Think Thin. The strategy provides higher stabilized module power, and significantly increases the throughput using thin cells. The 2nd generation ThinFab (ThinFab™140), presented at the World Future Energy Summit 2012, boasts a CAPEX
below $1.4/W_p$ (approx. $0.97/W_p$ for integrated end-to-end manufacturing line at 140MW).

This represents a production cost of only $0.48/W$, and electricity generation costs of $0.10/kWh [457], while providing a decent efficiency of 10.8%. In fact, a very attractive system cost of $1.4/W_p$ (ground mounted system) in China has been claimed, which shows enormous potential in other (sunny) developing countries such as India, Brazil, South Africa, etc. In this context, industries are now looking for new cell designs (and not an incremental progress in efficiency) to substantially decrease the tact time.

Fig. 63 Efficiency (initial) and current density per thickness of various one dimensional structured a-Si:H solar cells compared to the record stabilized a-Si:H cell [449] on random textured surface. Cell no. 1-9 (9 as reference cell) and the corresponding references are mentioned in Table 3. Tandem cell (no. 10 in Table 3) is not mentioned in this figure. The cells are electrically thin optically thick. Thickness of the absorber layer is smaller than the diffusion length; this ensures collection of carriers at the contacts avoiding recombination. Anti-reflection at the top surface and increased absorption due to light trapping in the nanorod arrays result in current enhancement. The efficiency is still small compared to standard [449] cells on textured surface, mainly due to low $V_{oc}$ and fill factor resulting from non-conformal growth on the nanorods, especially on sidewalls, leading to porous regions and shunt paths.
Researchers are now responding to that call by introducing extreme thin cells using the concept of electrically thin optically thick absorber layers. There are essentially two types of proposed structures, viz. nanorods [524,525,526] and nanoholes [527,528]. In the first category, a number of reports are now available with different nomenclatures—nanopillar [529], nanodome [530], nanorod [524], and nanocoax [531] etc. These types of structures have been made by either top-down or bottom-up approaches. The details of top-down/bottom-up growth method can be found in Ref. [16] and Sec. 12. The top-down approach is suitable for c-Si rod cells. Si nanowire solar cells are made by etching of c-Si substrates by chemicals [532] or plasma (RIE), and a conversion efficiency reaching 10% [533] has been achieved. However, bottom-up approach with metal induced c-Si nanorod solar cells have also been demonstrated [534]. For a-Si:H type of cells, on the other hand, a bottom-up approach is more suitable. Normally a seed layer is used, and the columnar growth occurs via a combination of mechanisms, viz. preferential direction growth, and growth on a catalyst seed. A typical catalyst method uses precipitated metal, such as gold induced vapor–liquid–solid (VLS) growth process [535,536]. In this VLS process, gold film (3-5 nm) deposited onto c-Si wafer is heated to form Au-Si alloy islands (droplets). When exposed to source gas (e.g. SiH₄), these islands decompose source gas, and Si diffuses into droplet and absorbed. After supersaturation, Si precipitates and SiNW grows out of precipitation [16].

Using Sn catalyst, an efficiency of 5.6% has been reported for a radial junction p-i-n a-Si:H solar cell on p-type c-Si nanowire [537]. Creating such structures directly on the substrate (such as glass) is an option.
Table 3 Thin-film Si cells on one dimensional structures. The efficiency of cells on nanoholes or nanorods have still not reached the efficiency of cells on standard (~10%) textured surface [449]. However, cells with absorber thickness below 100nm, even as small as 25nm are encouraging. This is possible due to flexible structure of amorphous material to form homogeneous coating (though still not fully conformal) on these high aspect ratio structures. The structures are made either by top-down (etching) or bottom-up (deposition) approaches.

<table>
<thead>
<tr>
<th>Cell No.</th>
<th>Cell type</th>
<th>Substrate</th>
<th>Intrinsic layer thickness (nm)</th>
<th>Source</th>
<th>Current density (mA/cm²)</th>
<th>Eff. (%)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>n-i-p (a-Si:H)</td>
<td>Nanodome</td>
<td>280</td>
<td>Stanford University, USA</td>
<td>17.5</td>
<td>5.9</td>
<td>[538]</td>
</tr>
<tr>
<td>2</td>
<td>n-i-p (a-Si:H)</td>
<td>Nanorod</td>
<td>25</td>
<td>Univ. Utrecht</td>
<td>8.3</td>
<td>3.6</td>
<td>[525]</td>
</tr>
<tr>
<td>3</td>
<td>n-i-p (a-Si:H)</td>
<td>Nanocoax</td>
<td>90</td>
<td>Stanford University+Solasta Inc.+EPFL(IMT), Neuchatel</td>
<td>13.9</td>
<td>8.2</td>
<td>[539]</td>
</tr>
<tr>
<td>4</td>
<td>n-i-p (a-Si:H)</td>
<td>nano cone</td>
<td>250</td>
<td>Stanford University/EPFL(IMT), Neuchatel/</td>
<td>14.9</td>
<td>9.7</td>
<td>[540]</td>
</tr>
<tr>
<td>5</td>
<td>p-i-n (a-Si:H)</td>
<td>nanotube</td>
<td>185</td>
<td>Stanford University, USA</td>
<td>13.5</td>
<td>6.1</td>
<td>[531]</td>
</tr>
<tr>
<td>6</td>
<td>p-i-n (a-Si:H)</td>
<td>nano cone</td>
<td>130</td>
<td>IBM T.J. Watson Research Center, USA</td>
<td>12.6</td>
<td>7.6</td>
<td>[541]</td>
</tr>
<tr>
<td>7</td>
<td>p-i-n (a-Si:H)</td>
<td>nanorod</td>
<td>300</td>
<td>Carl von Ossietzky University Oldenburg, Germany/University of Bremen, Germany</td>
<td>11.0</td>
<td>6.7</td>
<td>[526]</td>
</tr>
<tr>
<td>8</td>
<td>p-i-n (a-Si:H)</td>
<td>Plasmonic nanoprint</td>
<td>90</td>
<td>Univ. Utrecht/AMOLF</td>
<td>16.94</td>
<td>9.6</td>
<td>[542]</td>
</tr>
<tr>
<td>9</td>
<td>p-i-n (a-Si:H)</td>
<td>Random textured surface</td>
<td>250</td>
<td>EPFL</td>
<td>17.28</td>
<td>10.09</td>
<td>[449]</td>
</tr>
<tr>
<td>10</td>
<td>p-i-n Tandem (a-Si:H/ nc-Si:H)</td>
<td>Nanohole (Swiss Cheese)</td>
<td>-</td>
<td>Institute of Physics, Prague+Oerlikon Solar-Lab, Switzerland</td>
<td>10.0</td>
<td>10.3</td>
<td>[528]</td>
</tr>
</tbody>
</table>

Table 3 shows the performance of these one dimensional (1D) cells from different laboratories. Figure 63 shows the current density and efficiency per thickness of such cells compared to that in a standard cell structure [449]. The expected high stability of these cells...
against light soaking has, however, not been demonstrated yet and making conformal growth on such 1D structure remains a technological challenge.

7.6.2 Flat cells

In order to improve light trapping without macro or microscopic textures that generally lead to defects in the layers grown on them, electrically flat optically rough surfaces have been developed [543]. Flat cells employing a structure of mixed materials of different refractive indices, called flattened light-scattering substrate (FLiSS), have been demonstrated [544] in a nc-Si:H cell (Fig.64). The efficiency obtained for a nc-Si:H cell on FLiSS is comparable to that on a textured surface (efficiency ~8%), however, the $V_{oc}$ and FF are substantially improved. Further improvement in FLiSS is needed to enhance the current to make it comparable or higher than that is obtained on textured surface.

Fig.64  Schematic of a FLiSS (flattened light-scattering substrate or FLiSS) solar cell structure demonstrated in a nc-Si:H cell [544]. In this type of cells, mixed materials with different refractive indices are used. The substrate is a flattened light-scattering substrate, with a high reflective index contrast consisting of two dimensional ZnO grating filled with n-a-Si:H. For a nc-Si:H cell, the FLiSS structure provides substantial improvement in the infrared region (almost comparable to textured surface), while maintaining high $V_{oc}$ and fill factor, which can be obtained only on flat surfaces. With permission from [544], H. Sai, Y. Kanamori, and M. Kondo, Flattened light-scattering substrate in thin-film Si solar cells for improved infrared response, Appl. Phys. Lett. 98 (2011) 113502. Copyright © 2011 American Institute of Physics. License number 3513100577119.

7.7 Industrial competitiveness

One of the industrial successes of a-Si:H is large-scale displays, especially in the 1990s when Si based thin-film PV was in an initial phase. The processing technologies of these large area devices on glass substrates, and the roll-to-roll fabrication on flexible foils have been the main arguments in favor of thin-film Si PV. Applied Materials’ SunFab with
5.7 m² substrate was rolled out to many factories - Moser Baer in India, Signet Solar and SunFilm in Germany, Masdar Solar in UAE, T-Solar in Spain, Best Solar in China and Green Energy Technology in Taiwan. The strategy was that large glass would mean faster throughput, with fewer pieces delivering the same capacity, lowering the cost per watt, installation costs and BOS savings. As per experience from LCD-display industry, Applied Materials had seen that every time the glass grew larger, the industry was able to cut costs dramatically. However this strategy turned out to be a mistake for PV. A SunFab factory costs about 30% more than standard solar manufacturing equipment- $80 million to $160 million price tag for a single line. Glass this large is hard to handle, and few equipment manufacturers had tools that could deal with it. Signet, Sunfilm, Green Energy Technology and T-solar became bankrupt. Most SunFab owners ended up selling largely ¼ sized panels that were the same size as typical solar panels. In contrast, the competitor, Oerlikon company was more successful, selling a robust technology on an easily processable substrate (1.4 m²), and a high-efficiency double-junction cell processing at a high growth rate, due to its VHF technology. However, in the meantime TEL Solar has discontinued the solar business since 2014 and many of industries with TEL Solar/Oerlikon equipments have applied for insolvency- GADIR Solar, S.A in Spain, Pramac in Switzerland (30MW end-to-end turnkey line), Inventux in Germany, Auria Solar in Taiwan, Schuco Solar in Germany (Oerlikon and Applied Material SunFab) and Bosch Solar in Germany (30MW).

Roll-to-roll (R2R) technology on flexible substrates has so far shown the best promise. However it faces stiff commercial and technological challenges. A lower CAPEX, high-throughput, and simple processing are needed, particularly for low-cost encapsulation that should have the moisture barrier property comparable to that of glass. Recent reports show that using a multilayer of inorganic and organic materials made by same hot-wire CVD technique results in a water vapor transmission rate of $5 \times 10^{-6}$ g/m²/day at a temperature of
60°C and a relative humidity of 90%, which will increase the life time of PV to >30 years [545]. Nuon (the technology previously owned by Akzo Nobel) had to abandon their indigenously developed R2R technology (Helianthos concept) as it could not commercialize the product and the new owner of this technology HyET Solar is precisely putting its effort to make the technology cost-effective.

Though thin-film Si PV manufacturing is currently passing through a trying phase, the processing has matured, and fast multi-GW large-scale manufacturing is possible once the bubble of low priced c-Si sector has deflated. Moreover, the problem of light induced degradation that bothered the industries and investors, has been largely overcome. Applying all the new developments, such as thin cells, stable materials, and multi-junction, a degradation of as low as around 4% has been achieved by Unisolar [502].

7.8 Looking towards future: Bridge to third generation PV

In order to cross the S-Q limit of solar cell efficiency, several third generation PV concepts, most of which are still in conceptual phase, have been proposed [546]. The idea is to increase the efficiency to around 40-60% while keeping the cost of production low by using thin-films PV fabrication process. A few of these concepts, most relevant to thin-film Si, are described below.

7.8.1 Hot Carriers

The importance of thin absorber layer in PV cost reduction was discussed in Sec. 7.6.1. One more advantage of this structure is the ability to use a third generation concept of tapping the hot carriers before they thermalize, which is caused by phonon interaction in the lattice. This process can substantially increase the $V_{oc}$. The underlying principle of this type of solar cell is to slow down the rate of relaxation of photoexcited carriers, which is achieved by a quantum dot (QD) Si absorber layer, to allow time for carriers to be collected while they are still at high energies. The collection of carriers is through a selective (narrow) energy
contact, which can be achieved by single (doped) layer of Si QD providing the resonant level through which carriers can tunnel. A theoretical efficiency of 65% under 1 sun can be achieved by this solar cell design.

Fig. 6.5 Schematic diagram of proposed quantum dot triple-junction solar cell [547]. The doped layers can be standard amorphous and microcrystalline thin-films. The Si quantum dot layers can be made either by deposition of nanoparticles from gas phase by various PECVD processes, or by annealing (solid phase crystallization) of amorphous materials (α-SiC_x, SiN, α-SiO_x) at high temperature. Monodispersed (<5% size distribution) Si nanoparticles of size less than the Bohr’s radius (5nm) are embedded in an amorphous matrix (which acts as a passivation layer in addition to its role in quantum confinement) with spacings that allow current tunneling. Fully quantum dot cells can be made by using SiGe quantum dot, instead of the conventional c-Si wafer as the bottom cell. Bandgap is varied by tuning the quantum dot size. Reprinted with permission from [539], G. Conibeer, Si and Other Group IV Quantum Dot Based Materials for Tandem Solar Cells, Energy Procedia 15 (2012) 200. Copyright © 2014 Elsevier B.V. License number 3513101114061.

7.8.2 Quantum dots

One very promising outcome of the thin-film Si research is the material in which nanocrystallites are embedded in an amorphous matrix with 50% crystalline volume fraction that leads to high-efficiency nc-Si:H solar cells. This trend can be developed further by shrinking the size of the nanoparticles, below the Bohr’s radius, and thereby using quantum confinement. The resulting QD will be a milestone for third generation solar cells where the various properties of QDs such as decoupling of the electronic states from lattice, discrete electronic states, direct bandgap nature of light absorption, tuning the bandgap and absorption profile by tuning the particle size can be exploited. Though a multi-junction structure has been proposed in the third generation concept, this has been used for thin-film Si over a long time; in labs and commercial companies triple-junctions using a-Si:H, a-SiGe:H and nc-Si:H
have been made. However, even in lab scale the efficiency has not reached the S-Q limit. It is expected that the QDs are internally defect free and their surfaces can be passivated using appropriate shell or embedding in a passivating matrix. This way, bandgap variations can be made (by appropriate dot size) without increase of defects, which is encountered when changing bandgap with alloying such as a-SiGe or a-SiC. Figure 65 shows the schematic of a triple-junction based on QD layers. A theoretical efficiency of 47.5% for such a cell is expected [546]. Notwithstanding the advantages, the reports so far on solar cell devices with QDs have not proved their potential. A c-Si/QD-Si heterojunction cell has shown a reasonable \( V_{oc} \) of 0.52V, but a very low fill factor of 0.2. QD superlattice as intrinsic layer in an n-i-p cell has shown an efficiency of 3.8% with \( V_{oc} \), fill factor and \( J_{sc} \) of 518mV, 0.51 and 14.3 mA/cm\(^2\), respectively [548]. One of the causes behind the bad performance (in both c-Si/QD-Si heterojunction and QD superlattice as intrinsic layer in an n-i-p cell) is that in phosphorous-doped QD, the structural distortion is less significant than that for boron-doped case [549], and phosphorous-doping significantly increases the QD size compared to boron-doping [547]. Defect passivation of the QDs is still an open question. Si QDs have also been employed in QD sensitized solar cells whose theoretical efficiency is 44% [550].

Fig.66 Schematic diagram of a single-junction a-Si:H cell with upconversion layer [551]. The TCO layers have to be highly transparent for near-infrared photons (lowly doped), highly conductive (high mobility) and thick to minimize resistance losses. A non-conducting diffuse back reflector (white paint or foil) instead of Ag is used. Upconverter powders (e.g. NaYF\(_4\): 2% Er\(^{3+}\), 18% Yb\(^{3+}\), dissolved in chloroform with Poly(methyl
methacrylate)) can be drop casted on the back contact. A high bandgap layer with small sub-bandgap absorption
is the most suitable absorber (intrinsic layer) for upconversion cell. This concept is more suitable for high
bandgap absorber materials. Sub-bandgap photons are transmitted through the high bandgap absorber material
used in the cell, and are not utilized for electron-hole pair creation. In upconversion process, two below bandgap
energy photons (transmitted through the cell) are added by the upconversion layer and converted to a single
photon with higher energy and then reflected back to the bulk of the cell for absorption [15].

7.8.3 Up conversion

Light spectrum below the bandgap is lost in a solar cell and this long wavelength
spectrum can be converted to above bandgap, thereby utilizing a part of the unused light.
This third generation concept will be most useful for high bandgap absorber materials where
there is a substantial transmission loss, and a-Si:H, especially the pc-Si:H type cell, is a test
case because of its high bandgap of 1.8-2.0eV [551] (Fig. 66). Using lanthanide type up-
converter materials, up-conversions have been achieved for broad band light. However, for a
realistic improvement, a concentrated light of ~500 suns is needed. Use of up-conversion
based on sensitized triplet–triplet-annihilation in organic molecules at the back side of a-Si:H
cell has shown 1% increase in efficiency at 48 suns illumination [552]. However, a solid state
material by a deposition technique is most desirable. One of the solutions to capture a wide
spectrum by a broad band absorption can be achieved by using quantum dot sensitizers or
transition metal ions, which emit at the resonance energy of the up-converter. The latter
(transition metal ions) is yet to be experimentally successfully demonstrated, but the former
has shown promise; QDs absorb over a broad spectral range in the IR, and emit in a narrow
line, e.g. around 1520 nm, resonant with the \( \text{Er}^{2+} \) upconversion wavelength to which it makes
a radiative transfer [553]. Use of plasmonic structure to either increase the absorption
strength or emission has also been proposed and has also been shown as proof of concept.
One more technique is to use nanofocussing to achieve the light concentration. This can be
done externally using nanolenses, or internally through nanafocussing at a tapered metallic
structure at its edge [554].
7.9 Future outlook

Thin-film Si based PV technology, like all other thin-film technologies, will continue to face commercial pressure from Si wafer based PV for some time to come and will mostly cater to the niche market. These include small power sources in consumable goods, in addition to a dedicated market in building integration, thanks to its aesthetics. Once the dominance of c-Si PV eases, thin-film Si PV technology market is expected to expand rapidly, as this is the most matured and robust technology positioned to upscale. Gigawatt level production is possible with its technology with relatively small effort. In this regard, the large display size solar panels and long rollable modules will be preferred choices because of the maturity of the fabrication process and technology.

As far as absorber material is concerned, a new direction on deposition/fabrication is needed. At present, the stabilized efficiency of single-junction cells, whether a-Si:H or nc-Si:H, is far below (less than half the S-Q limit) the theoretical optimum efficiencies for the respective band gaps. The stabilized efficiencies of even triple-junction cells are around one third of the theoretical efficiency of multi-junction. However, considering the enormous room for improvements in defect density, mobility, etc., considerable scientific interest remains for long-term efforts. Production of nanowires and quantum dots will be of enormous scientific interest, however, multi-junction solar cells based on quantum dots, notwithstanding their potential for high-efficiency beyond S-Q limit, will remain academic for some time to come, just as other third generation concepts.

In terms of industrial production, a-Si:H will remain central to SHJ type solar cells. However, as far as pure thin-film Si PV is concerned, there are challenges ahead. There are ongoing efforts on implementing these type of cells along with others to fabricate parallel connected (e.g. two terminal devices with optical couplers or honeymoon cells) devices. The previous decade had experienced great success in developing the passive parts of thin-film Si
cells, especially optical management and light trapping effects, which included nano-textured surfaces, nanowall/nanopillars and plasmonic effects. Many of these were developed by groups specializing in optical studies, not necessarily experts in solar cells and device fabrication. The knowhow of many of these effects is currently being incorporated in solar cells. Industrial fabrication processes implementing these optical enhancing effects may soon be developed. This will be the best possible way to increase stabilized cell efficiency to 15%, which will make the thin-film Si based PV truly industrially competitive. The solar cells on flexible foils, especially plastics, still remain one of the most fascinating inventions in thin film silicon based solar cells. It is to be seen how low-cost encapsulating moisture barrier layers develops in near future to make the plastic solar cells a real success, opening up applications in wide ranging areas, especially large roof tops.

## 8.0 CZTSSe (Kesterite) Solar Cells

The desire for large-scale PV technology based on environmentally friendly, low-cost absorber compatible with high-throughput fabrication has resulted in an increased research interest in the kesterite-type Cu$_2$ZnSn(S,Se)$_4$ systems known as CZTS (or CZTSSe in some cases when Se is present). With similar optoelectronic properties to high-efficiency CIGS and CdTe materials, and at the same time devoid of highly toxic (such as Cd) and high-demand rare elements (such as indium), this material has produced solar cells with steadily increasing efficiency during the recent years [555]. Remarkably, CZTSSe progress has been accelerated by chemical ink-based approaches surpassing in performance classical high-vacuum techniques and pushing the efficiency record of these materials by about 1 absolute % per year up to its current level of 12.6% [556-559]. The combination of these advantages together with a huge potential for improvement has motivated an expanding volume of studies, ranging from kesterite synthesis to advanced materials and device modeling. A number of detailed works have already provided exhaustive coverage of the significant body
of literature on the subject [555,560,561]. Here we will focus on the key aspects of CZTSSe material and device developments during the recent years, analyzing the main challenges ahead of currently one of the most tempting and complex PV absorber materials.

### 8.1 CZTSSe materials

Copper zinc tin sulfide (Cu$_2$ZnSnS$_4$) was conceived in the 1980s as a promising PV material to provide alternative to indium-based chalcopyrites such as CuInSe$_2$ and later Cu(In,Ga)(S,Se)$_2$ that at the time were reaching 11% efficiencies, close to the 2013 efficiency values of CZTSSe devices [562]. The material comprises a next level of evolution of the adamantine (i.e. diamond-like) family of analogous structures where 4-valence atoms are consecutively substituted with isoelectronic combinations of growing complexity, for example [563], carbon (or Si) $\rightarrow$ ZnS $\rightarrow$ CuInS$_2$ $\rightarrow$ CuZnSnS$_4$ (Fig.67). The substitution of indium (III valence) in the chalcopyrite with Zn (II valence) and Sn (IV valence) in kesterite results in very similar optoelectronic properties – i.e. high absorption co-efficient due to direct bandgap, tunable from approximately 1eV to 1.5eV with varying S/Se ratio, the lowest values corresponding to pure selenide and the highest to pure sulfide materials.

![Fig. 67 Schematic diagram of a part of the adamantine compound family, including kesterite materials. Isoelectronic combinations of different atoms are substituting Roman numbers indicate the valence state of the cations (big spheres A,B,C) and anions (small spheres) respectively. The sum of the valences at each step is double the sum of the previous. The structure models at the left side are (from top to down) the sphalerite-type structure, the chalcopyrite-type structure and the stannite-type structure. CZTS is a kesterite material used as absorber in the CZTS solar cell due to its high absorption co-efficient, optimum bandgap of around 1.5eV, and its elemental constituents are earth-abundant. Reprinted from Ref. [563], S. Schorr, Structural aspects of](image-url)
The dilemma whether to use the classical sulphide or selenide or mixed materials is similar to that in chalcopyrite technology. On the one hand, sulfur is more benign and orders of magnitude more Earth-abundant than Se – therefore the natural choice for large-scale environmentally friendly manufacturing. On the other hand, Se-based materials produce higher-quality polycrystalline layers and are more tolerant to processing conditions. Neither long-term availability of Se nor its potential toxicity has yet been viewed as a major limiting factor for the growth of PV technologies employing it. Se is a largely unused byproduct from Cu refining and, although harmful in excessive concentrations, is a key micronutrient for living organisms. An important advantage of mixed sulfoselenide alloys is the ease of controlling the bandgap from about 1eV (pure selenide) to about 1.5eV (pure sulfide) analogously to CuIn(SSe)₂. The use of the pentanary Cu₂ZnSn(S,Se)₄ system allows to take advantage of the optical and materials quality benefits of the combination of S and Se and has been employed in the highest-efficiency CZTSSe devices to date [558,559].

The high complexity of the kesterite materials makes them particularly vulnerable to secondary phase formation – a major challenge for the fabrication of high quality absorbers. The high temperatures (over 500°C) required for device-quality kesterite film crystallization [564,565] combined with the high volatility of multiple intermediate species are a serious challenge [566] for CZTSSe (not only S and Se as in CIGS technology, but also of elemental Zn and Sn chalcogenide phases). Materials optimization is made even more difficult by the fact that the two of the most likely secondary phases, viz. Zn(S,Se) and Cu₂Sn(S,Se)₃ are difficult to distinguish by standard characterization techniques such as x-ray diffraction (XRD) due to peak overlap with the targeted CZTSSe. Raman scattering [567,568] and other techniques such as neutron diffraction [569] and x-ray absorption near edge structure [570,571] have been successfully used for phase detection, although there is still a need for...
Further development of techniques for routine and reliable secondary phases detection in CZTSSe, especially in the pentanary system.

Some secondary phases can be more detrimental than others. Generally, secondary phases with bandgaps lower than CZTSSe (for example Cu$_2$Sn(Se)$_3$, bandgap of 0.8-1eV), are considered particularly undesirable as they reduce the V$_{oc}$ of the device. It has been pointed out that the presence of a material with a bandgap lower by only 100meV will reduce the maximum achievable efficiency by 8% absolute [561]. High-conductivity phases, such as Cu$_x$(S,Se) are especially damaging performance well due to their shunting effect. Similarly to chalcopyrite PVs employing CIGS or CuInS$_2$, they must be avoided by relying on a Cu-poor absorber or removal techniques such as potassium cyanide (KCN) etch [572,573].

Phases with higher bandgap than CZTSSe are considered less detrimental [561] but may have negative impact in specific locations – for instance Zn(S,Se) (bandgap of 2.7-3.8eV) in the bulk of the film is much less harmful than on the absorber surface [574]. HCl etch has been successfully applied to remove surface Zn excess leading to improved V$_{oc}$ [575]. Tin chalcogenides, Sn(S,Se), may have different impact depending on exact composition, while SnSe has a relatively high bandgap of 1.3eV and may have little effect on device performance, SnS has an indirect bandgap of 1eV and can be potentially harmful [561]. This could be one of the reasons why pure sulphide CZTSSe has lower maximum efficiency than materials with higher Se content.

All above considerations are in empirical agreement with the currently best strategies for high-efficiency devices that employ mixed S-Se materials with slightly Zn-rich and Cu-poor composition [558,559].

### 8.2 Fabrication approaches

Numerous vacuum and non-vacuum CZTSSe fabrication approaches have been reported [555,556,572,576,577]. One distinguishing property of these materials is Sn-
chalcogenide volatility, especially at high-temperature and in vacuum. This has made direct process such as co-evaporation at high substrate temperature very difficult to optimize CZTS films, which was possible with CIGS. Currently, the most successful CZTSSe fabrication processes are two-step vacuum and non-vacuum deposition techniques where the high-temperature (over 500°C) crystallization step is done at atmospheric pressure.

The first report on the deposition of CZTSSe films by employing sputtering from quaternary targets and its use in PV device was performed by Ito and Nakazawa in 1988 [562]. Katagiri et al. [578] employed sputtering from metal targets to systematically study an extensive matrix of composition and processing parameters. Careful optimization determined the beneficial Cu-poor, Zn-rich composition, and with the demonstration of 5.75% efficiency in 2007 [579] that was increased later to 6.8% by simple wet etching technique [555,580], triggered a rapid growing research interest in CZTSSe PV. Among numerous other reports on sputtering, the company Solar Frontier has reported the highest efficiency of 9.2% that was furthermore measured over the total area of a 25cm² mini module [581].

Co-evaporation at high substrate temperature was the technique used for the first time to demonstrate over 2.3% efficient CZTSSe solar cell in 1997 [566] at the University of Stuttgart, highlighting for the first time the Sn-loss challenges mentioned above. Fast co-evaporation helped mitigate this issue and increase the efficiency to 4.1% [582]. Recently the National Renewable Energy Laboratory team was able to adapt their high-performance CIGS co-evaporation process to CZTSe, reaching 9.2% efficiency by maintaining temperatures no higher than 500°C and providing higher Sn flux throughout the whole process [583]. The same group reported that, similarly to CIGS, Na incorporation in CZTSe has strong impact on the electronic properties [584]. Successful grading of the composition to create advantageous bandgap profile similarly to highest performance co-evaporated CIGS has not been reported yet.
Sequential processes based on evaporation at relatively lower temperature (<200°C) followed by high-temperature (>500°C) crystallization step have also lead to successful CZTSSe developments. The first one in this category was reported in 1997 by employing 500°C sulfurization of Zn/Sn/Cu stacks. It yielded 0.66% efficiency [585], which was later improved to 5.45% by Na incorporation together with optimization of other parameters [586]. The impact of Sn vapor pressure during the high-temperature crystallization step of CZTS precursors was demonstrated by using sealed-tube anneal with a small amount of Sn source, where an efficiency of 5.4% was observed [587]. The highest efficiency pure sulfide CZTS devices were developed at IBM by co-evaporation followed by anneal and have reached 8.4% [588]. Mixed sulfoselenides by a similar process have demonstrated 8.9% efficiency by use of TiN diffusion barrier at the back contact [576].

Electrodeposition is a mature industrial non-vacuum deposition technique, attractive for large-scale CZTSSe manufacturing. Single step and multi-step electrodeposition of CZTSSe thin-films have been reported [572,573,589,590]. Stacked metal precursor layers, subjected to sulfurization and KCN etch yielded 3.2% efficiency [572]. Co-electrodeposited Cu-rich metal precursors, with KCN etching to remove copper sulfide reached 3.4% [573]. IBM process based on electrodeposition of stacked elemental layers with subsequent sulfurization has reached 7.3% efficiency [590].

Ink-based fabrication processes are compatible with ultrahigh-throughput fabrication techniques such as printing and casting. Different ink approaches based on solutions, nanoparticle suspension and mixed solution-nanoparticle slurries could offer unprecedented scaling potential to CZTSSe.

The first report on nanoparticle CZTSSe deposition involved hot reaction in ethylene glycol [591]. Guo et al. [592] employed higher-temperature hot injection in oleylamine, and achieved 7.2% efficient devices. This value was later increased to 8.5% by use of binary zinc...
sulphide (ZnS) and ternary copper tin sulphide (Cu₂SnS₃) particles that were subjected to selenization [593]. Hybrid solution-nanoparticle slurries in hydrazine based on dissolved Cu-Sn-S-Se systems and dispersed Zn-Se phases were developed at IBM, and reached a breakthrough 9.66 % efficiency in 2010 [556]. The method was further improved to yield 10.1% [557] and recently achieved CZTSSe efficiency of 11.1% [558]. Figure 68 shows the pinhole-free large-grained microstructure of these materials. The absorber thickness is close to 2 µm and the elemental distribution measured by energy-dispersive x-ray spectroscopy (EDX) is flat across the film. It must be noted that contrary to CIGS, with CZTSSe no reports on successful elemental grading targeting bandgap engineering for enhanced efficiency has been reported to date. This however, as will be shown below, is not the main performance-limiting factor so far, as efficiencies over 15% [594] have been achieved with CIGS even with flat elemental profiles.
Pure solution inks potentially have advantages for uniform synthesis of multinary compound layers over particle-containing systems due to greater homogeneity at a molecular scale, as well as reduced probability for aggregate formation causing coating defects. Pure solutions of metal salts and thiourea in dimethyl sulfoxide have been used to achieve 4.1% efficient devices [595]. CO$_2$ solutions in hydrazine (forming hydrazinocarboxylic acid) were successfully used to dissolve Zn species in hydrazine-based inks, yielding 8.1% efficient devices [593]. Another pure solution approach for hydrazine systems based on substitution of elemental Zn with Zn salts was developed with reported efficiency of 10.6% [596].

### 8.3 Device Characteristics

Here, we review device characteristics of the high performing CZTSSe cell and benchmark it against the high performing CIGSSe cells, as well as a hypothetical S-Q single-junction solar cell (S-Q limit cell) to understand the key problems in the current generation of CZTSSe cell. We will discuss the general device characteristics of CZTSSe (Sec.8.3.1), including the $V_{oc}$ deficit issue (Sec. 8.3.2), which is among the leading challenges facing CZTSSe technology.

#### 8.3.1 Electrical Characteristics

Figure 69 shows the (a) J-V curve, (b) IQE and photoluminescence (PL) spectra of CZTSSe and CIGSSe solar cells. Table 4 shows the J-V characteristics of an example of leading CZTSSe (IBM-CZTSSe) device with efficiency of 11.1% [558], the leading CIGSSe cell (20.3% efficiency) from Zentrum für Sonnenergie-und Wasserstoff-Forschung (ZSW), Germany [597] and the S-Q limit cell with the same bandgap (1.13eV) (similar discussions will also apply to the current CZTSSe record efficiency of 12.6%). This S-Q limit cell presents the ultimate limit of a single-junction solar cell based on S-Q limit calculation
In Table 4, we also present electrical characteristics of a high performance CIGSSe cell (IBM-CIGSSe) with 15.2% efficiency made by analogous hydrazine-based processing [594]. The bandgap in these cells are determined from the inflection point (i.e. the maxima of $|dQE/d\lambda|$ curve) of the QE curve near the bandgap cut-off wavelength [599]. In order to perform a fair comparison of $J_{sc}$ and $V_{oc}$ among these cells with little variation in bandgap, $V_{oc}$ deficit value, i.e. $V_{oc\,def} = E_g/q - V_{oc}$ and normalized $J_{sc}$ value, i.e., $J_{sc,N} = J_{sc}/J_{sc,\,\text{MAX}}$ where $J_{sc,\,\text{MAX}}$ is the $J_{sc}$ of an S-Q limit cell or the maximum $J_{sc}$ assuming a 100% EQE, are monitored.

![Fig. 69](image-url)  
(a) J-V characteristics of IBM-CZTSSe, ZSW-CIGSSe leading cells, and a S-Q limit cell with similar bandgap (1.13 eV). The S-Q limit is calculated for a single-junction cell with AM1.5G illumination. (b) Internal quantum efficiency and the photoluminescence spectra (red curve) at room temperature of the 11.1% IBM-CZTSSe [558] and the 15.2% IBM–CIGSSe cells [594]. The bandgap (marked as $E_g$) is determined from the inflection point (or the maximum slope) of the external quantum efficiency curve. Fig. 69 (b) reproduced from Ref. [600], Tayfun Gokmen, Oki Gunawan, Teodor K. Todorov and David B. Mitzi, Band tailing and efficiency limitation in kesterite solar cells, Appl. Phys. Lett. 103 (2013) 103506. Copyright © 2013 AIP Publishing LLC. Permission granted.

**Table 4.** Device performance of leading CZTSSe and CIGSSe (from IBM and ZSW respectively) based solar cells. The parameters $R_{SL}$, $A$, and $J_0$ respectively are series resistance under light, diode ideality factor and reverse saturation current determined using Sites’ method [601]. $J_{sc,N}$ and $V_{oc,\,\text{def}}$ are normalized $J_{sc}$ and $V_{oc}$ deficit, respectively (see text).
### Table 1: Performance Parameters of Various Solar Cells

<table>
<thead>
<tr>
<th>Solar cell</th>
<th>Voc (V)</th>
<th>Jsc (mA/cm²)</th>
<th>Fill factor</th>
<th>Eff. (%)</th>
<th>Eg (eV)</th>
<th>Jsc,N (%)</th>
<th>Voc,def (V)</th>
<th>Rsl (Ω)</th>
<th>Area (cm²)</th>
<th>J0 (mA/cm²)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>IBM-CZTSSe</td>
<td>0.460</td>
<td>34.5</td>
<td>69.8</td>
<td>11.1</td>
<td>1.13</td>
<td>79.5</td>
<td>0.670</td>
<td>0.40-0.60</td>
<td>1.48</td>
<td>1.34x10⁻⁴</td>
<td>[558]</td>
</tr>
<tr>
<td>IBM-CIGSSe</td>
<td>0.623</td>
<td>32.6</td>
<td>75.0</td>
<td>15.2</td>
<td>1.16</td>
<td>78.2</td>
<td>0.547</td>
<td>0.75</td>
<td>1.49</td>
<td>9.8x10⁻⁶</td>
<td>[594]</td>
</tr>
<tr>
<td>ZSW-CIGSSe</td>
<td>0.730</td>
<td>35.7</td>
<td>77.7</td>
<td>20.3</td>
<td>1.14</td>
<td>83.2</td>
<td>0.410</td>
<td>0.23</td>
<td>1.38</td>
<td>4.2x10⁻⁸</td>
<td>[597]</td>
</tr>
<tr>
<td>SQ 1.13 eV</td>
<td>0.883</td>
<td>43.4</td>
<td>87.2</td>
<td>33.4</td>
<td>1.13</td>
<td>100</td>
<td>0.247</td>
<td>0</td>
<td>1</td>
<td>4.55x10⁻¹⁴</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 70 breakdown analysis of various loss mechanisms diagram of the 11.1 % CZTSSe cell [558] benchmarked against S-Q limit: (a) Voc, (b) fill factor (FF), and (c) Jsc. Voc deficit is the number one problem in CZTSSe technology and is mainly attributed to various non-radiative recombination, interface recombination, bulk recombination, back contact recombination and band tailing. The second dominant factor is the fill factor loss attributed to the Voc loss, and series resistance losses from various sources such as metal contact resistance, bulk resistance, potential barrier across the contact, and grain boundaries. For higher bandgap or higher [S]/[Se] ratio, series resistance tends to increase. The last and least loss factor is the Jsc loss which is attributed to the common loss factors in thin film solar cells.

We have performed a more detailed breakdown analysis of various loss mechanisms for the IBM-CZTSSe cell in the frame work of S-Q limit as shown in Fig. 70. The leading
CZTSSe cell has \( V_{oc} \) at 52.1%, fill factor at 80.0% and \( J_{sc} \) at 79.5% of the S-Q limit cell. It is clear that the \( V_{oc} \) deficit (Fig. 70 (a)) is the number one problem in the current generation CZTSSe. We will discuss factors that account for this \( V_{oc} \) deficit in more detail in later section.

Second issue is the shortcoming of fill factor. A majority of the fill factor loss is due to various sources of series resistances (Fig. 70b) that accounts for 9.4 % absolute from the of S-Q limit fill factor such as top metal contact resistance, bulk resistance across the film, current blocking secondary phase like ZnS(e) [602] and possible potential barrier contribution across back contact or grain boundaries [603]. Note that the CZTSSe series resistance tends to increase with higher bandgap, or with higher [S]/[Se] ratio. Overall, the series resistance of IBM-CZTSSe is comparable, even slightly better, than the analogous hydrazine-processed IBM-CIGSSe device (Table 4). The lowest series resistance (\( R_s \sim 0.2 \Omega \text{-cm}^2 \)) is found in selenide (no sulfur) kesterite CZTSe cell with lowest bandgap [583,604].

Another contribution of the fill factor losses is accounted by \( V_{oc} \) deficit loss [Fig. 70(b), 8% absolute the maximum fill factor], as low \( V_{oc} \) value also inadvertently drags down the fill factor. The maximum possible fill factor at a given \( V_{oc} \) can be calculated by the following phenomenological relationship [605]:

\[
\text{Fill factor} = \frac{[V_{ocn} - \ln(V_{ocn} + 0.72)]}{(V_{ocn} + 1)}, \text{ where } V_{ocn} \text{ is the normalized } V_{oc}, \text{ and}
\]

\[
V_{ocn} = \frac{qV_{oc}/Ak_BT}{}, \text{ with } q \text{ is the electronic charge, } A \text{ is the diode ideality factor, } k_B \text{ is the Boltzmann constant and } T \text{ is the temperature.}
\]

CZTSSe has a dramatically different temperature characteristics at low-temperature compared to that of CIGSSe. Figure 71(a) shows that the CZTSSe efficiency collapses at low-temperature (\( T < 150K \)) while in contrast the CIGSSe cell efficiency keeps increasing. The series resistance diverges as much as 100 times from 340K to 120K [603] as shown in
This causes a drastic collapse in fill factor, and correspondingly a decrease in observed efficiency [603,606]. This effect is suspected due to dielectric freeze out effect in the bulk CZTSSe [607] because of the absence of shallow acceptor in CZTSSe [607,608]. This is consistent with the theoretical calculation using density functional theory that suggests CuZn antisite as the dominant, deep acceptor defect in CZTSSe [608,609]. Bandgap dependence study indicates that this defect level increases with increasing bandgap or sulfur content [607,610]. An alternative view suggests the presence of secondary phase ZnS(e) at the absorber/buffer interface limits the transport across the cell and causes this divergence in series resistance [602].

The J_{sc} of IBM-CZTSSe cell is surprisingly very good, with J_{sc,N} value slightly better than that of the IBM-CIGSSe cell. This is most likely a fortuitous effect of the tail states in CZTSSe that extend the absorption below the CZTSSe bandgap [600]. The effect of the tail states is visible in the QE curve as shown in Fig. 69(b) where we observe more tailing in the CZTSSe QE curve around the bandgap cut-off wavelength. Several factors still affect the IBM-CZTSSe J_{sc} compared to the S-Q limit J_{sc}. These are shadowing loss of the top metal grid, reflection loss mainly from the top stack, absorption loss of the TCO and cadmium sulphide (CdS) layer and carrier collection losses in the bulk, which is apparent from lower QE response at long wavelength near the bandgap cut-off wavelength. Each of these components accounts for about 4-5% loss with respect to the maximum J_{sc}. 

![Graphs](image-url)
Fig. 71 Temperature dependence of (a) efficiency, and (b) series resistance under light condition of the IBM-CIGSSe versus IBM-CZTSSe solar cells. The measurement is performed in a liquid nitrogen cooled cryostat under simulated 1 sun AM1.5G illumination. CIGSSe cell efficiency keeps increasing even at low-temperature. Compared to CIGSSe, at low-temperature, CZTSSe has different temperature characteristics. Cell efficiency decreases rapidly at low temperature (<200K) which is related to the divergence in series resistance and drastic decrease in fill factor. This effect is attributed to the freeze-out effect in the CZTSSe absorber film due to the loss of free carrier at low-temperature which can be attributed to the deep acceptor level in CZTSSe. As can be seen in (b), CZTSSe series resistance diverges about 100 times from 340K to 120K.

8.3.2 The $V_{oc}$ deficit in CZTSSe

The high $V_{oc}$ deficit ($V_{oc,def} = (E_g/q)-V_{oc}$) is among the biggest challenges facing CZTSSe-based solar cell, and thus merits a special discussion. Several factors account for severe $V_{oc}$ deficit in CZTSSe solar cell. They can be categorized into two major loss components as shown in Fig. 70(a): (i) non-radiative recombination, and (ii) band tailing effect.

The majority of the $V_{oc}$ deficit loss is accounted for by non-radiative recombination (~25% of S-Q limit $V_{oc}$). Several factors contribute to this loss components, such as interface recombination (that may also induce Fermi level pinning at the interface) and bulk recombination due to electrically active defects and back contact recombination.

We study the $V_{oc}$ versus temperature characteristics of the CIGSSe and CZTSSe, as shown in Fig. 72. The activation energy of the dominant recombination process can be obtained (assuming a constant diode ideality factor) from the intercept of the $V_{oc}$ versus $T$ extrapolation line at 0K [603,611]. The IBM-CIGSSe cell has activation energy equal to the bandgap, as expected for a very good solar cell. However, the activation energy for CZTSSe falls short of its bandgap value. This behavior can be accounted by the two $V_{oc}$ deficit factors discussed above: (i) non-radiative interface recombination and its consequent Fermi level pinning behavior, and (ii) the effect of tail states that artificially lowers the bandgap of CZTSSe thus lowering activation energy [600].
Fig. 72 Temperature dependence of $V_{oc}$ for IBM-CIGSSe and IBM-CZTSSe solar cells. The intercept of the (extrapolated line at 0K) $V_{oc}$ versus temperature plot at 0K is the activation energy of the dominant recombination process. Activation energy is equal to the bandgap for the CIGSSe cell (and other ideal solar cells) while for CZTSSe activation energy is smaller than its bandgap. This is attributed to dominant non-radiative interface recombination, Fermi level pinning, and tail states that effectively reduces CZTSSe bandgap and activation energy.

There are several possible sources of severe interface recombination in CZTSSe solar cells, such as defective buffer-absorber interface or secondary phases like ZnS(e) [561] at the interface. Another possible source is a cliff-like band alignment where the conduction band of the CdS is lower than the absorber layer [612]. However an ultraviolet-photoelectron spectroscopy study on CZTSSe reveals the opposite, i.e. a spike-like band alignment in CZTSSe solar cell across all bandgap [613]. Separate study suggests that high bandgap (or full sulfur) CZTS has a cliff-like band alignment [614]. The discrepancy to earlier study [613] is suspected due to variation in sample preparation.

The second major factor that contributes to the $V_{oc}$ deficit in CZTSSe solar cell is the tail states that arise from electrostatic potential fluctuations induced by high concentration of native defects and strong compensation [600,615,616]. Temperature dependence study of time-resolved PL [676] and laser intensity dependence study [616] provide evidence that supports this potential fluctuation model. A thorough theoretical study by Chen et al. [617,618] on CZTSSe absorber revealed several major features in the electronics properties of CZTSSe, such as strong phase competition between the kesterites and secondary compounds, intrinsic p-type conductivity due to Cu$_{Zn}$ antisite, Cu vacancies and existence of
charge-compensated defect clusters such as [2CuZn + SnZn], [VCu + ZnCu] and [ZnSn + 2ZnCu]. These defect clusters contribute to the severe potential fluctuation in CZTSSe.

One evidence of the tail states effect in CZTSSe can be observed from the weak tail of the QE curve near the bandgap cut-off as shown in Fig. 69(b). Another evidence is found in the PL characteristics as shown in Fig. 69(b). CZTSSe PL peak occurs at lower energy values than its bandgap [561,600]. In contrast, the PL peak of CIGSSe is close to its bandgap values as expected for a high quality material [600]. This suggests that these tail states artificially lower the CZTSSe bandgap, thus in effect also lowering the $V_{oc}$ [600]. Furthermore lower dielectric constant ($\varepsilon_r \sim 7-8.5$) [607,619] in CZTSSe (compared to CIGSSe $\varepsilon_r \sim 12$) also causes more severe band tailing effect [600].

The CZTSSe bandgap, which can be controlled by the [S]/[Se] ratio, also plays an important role in the $V_{oc}$ deficit characteristics. We observe an efficiency versus bandgap profile that peaks around bandgap of 1.15 eV as shown in Fig. 73(a). We found that $V_{oc}$ does not increase at the same rate as the bandgap [e.g. see $(E_g/q) - 0.5V$ reference line for comparison in Fig. 73(b)]. In other words, the $V_{oc}$ deficit gets larger at larger bandgap or at larger [S]/[Se] ratio. Several factors can account for this behavior such as (i) a constant deep level defect at 0.8eV from the valence band detected by transient photocapacitance study [620], (ii) electron trapping [2CuZn+SnZn] defect clusters that becomes more abundant in CZTS (full sulfur) [617], and (iii) lower dielectric constant at higher bandgap [619] that leads to more severe tail states [600], (iv) more severe interface recombination at higher bandgap.

An increasing $V_{oc}$ deficit with bandgap is partly responsible to efficiency profile that peaks around 1.15eV bandgap as shown Fig. 73(a). Another factor that contributes to this behavior is increasing series resistance with bandgap [Fig. 73(c)] that lower the fill factor at high bandgap. Note that analogous effect of increasing $V_{oc}$ deficit and similar optimum bandgap around 1.15eV have also been observed in CIGSSe [621].
Fig. 7.3 Bandgap dependence characteristics of champion CZTSSe (circles) and CIGSSe cells (stars): (a) efficiency, (b) $V_{oc}$ and $(E_g/q) - 0.5V$ reference line, and (c) series resistance from light I-V. Empty circles are data point for the current CZTSSe champion [559]. Dashed curves are guide to the eye. For CZTSSe solar cell, efficiency peaks around 1.15eV and $V_{oc}$ does not increase at the same rate. $V_{oc}$ deficit becomes higher at higher bandgap is due to electron trapping defects, lower dielectric constant at higher bandgap, higher interface recombination at higher bandgap and increasing series resistance with bandgap.

8.4 Future direction

Over the past few years CZTSSe PV technology has experienced rapid growth both in conversion efficiency and materials understanding. These advances have been achieved by the collective effort of an expanding research community interested in this challenging and promising multinary material with yet unachieved efficiency potential. Future breakthroughs in fabrication strategies are expected to improve phase and electrical uniformity and address issues related to the main device limitations. The predominant problem is the $V_{oc}$ deficit, which is mainly attributed to the band tail states due to high concentration of native defects and strong compensation; and severe non-radiative recombination processes due to bulk defects and possible interface recombination. Fortuitously these tail states increase the sub-bandgap absorption that boosts the $J_{sc}$ and leads to surprisingly good $J_{sc}$ characteristics in CZTSSe solar cells on par with CIGSSe. An understanding and control over interface recombination and the defects that give rise to the tail states is needed to reduce the $V_{oc}$ deficit, and improve the performance of CZTSSe solar cells.

Several approaches can be pursued to reduce the $V_{oc}$ deficit such as:

(i) Alternative buffer engineering in attempt to increase the absorber interface quality or to alter the bulk property. Recently an In$_2$S$_3$/CdS double emitter structure has been shown to
yield a record $V_{oc}$ deficit in lower bandgap CZTSSe [622]. Some of the improvement is partly attributed to the effectiveness of indium doping to CZTSSe that helps increases the $V_{oc}$.

(ii) Focus on low bandgap (selenide) CZTSSe (~1.0 eV) to achieve better $V_{oc}$ deficit.

(iii) Effort to minimize the tail states by using alternative elemental substitutions.

9. Planar thin-film and nanostructured CdTe solar cells

While the first generation (1G, mainly Si based) solar cell manufacturing and installation costs are relatively low, the development of second generation (2G) thin-films polycrystalline solar cells still face higher costs compared to efficiency. Given that c-Si (commercial wafer thickness 180µm) based a-Si:H/c-Si solar cells have demonstrated 25.6% efficiency [484], while planar 2G CdTe solar cells (CdTe thickness ~2µm) have shown 22.1% efficiency [623,624], there is a scope for extensive research on CdTe based solar cells to bridge the difference. The schematic diagram of CdTe solar cell is shown in Fig. 74.

Considering that the major barrier for an ultra-large-scale use of solar energy is the high production cost and low efficiency of the solar cells, one may easily understand the importance of any investment in strategies to solve these drawbacks. Within this context, third generation (3G) nanostructured solar cell will play an important role in the future with the use of new strategies with a competitive efficiency that have been theoretically understood but experimentally not yet demonstrated.
In the above context, CdTe is an essential player in general in materials science, and in particular in the solar cell market, playing an important role both in planar 2G and nanostructured 3G solar cell where significant efforts are being currently undertaken both for enhancing efficiency and reducing costs. In fact, CdTe is an ideal absorber where 1µm thick 2G solar cell can absorb 90% of the solar spectrum with good conversion efficiency [30,625], considering a bandgap around 1.5 eV depending on the dopant used. Together with this, the use of simple and low cost manufacturing process makes CdTe based solar cell an extraordinary candidate in the photovoltaic field, with the production of commercial 2G modules of 16.1% efficiency and US $0.68/W obtained by First Solar [626,627]. This is still significantly less than the theoretically expected maximum value of 29% for CdTe solar cells [626]. Recently, an efficiency of 12% has been reported for nanostructured CdS/CdTe solar cells [628].
makes this material an ideal candidate for absorber, the review is focused on thin-films 2G, and nanostructured 3G CdTe solar cells.

9.1 Properties of materials used in CdS/CdTe solar cells

The materials used as front contact are transparent conductive oxides, i.e. materials that conduct electricity and also allow the light to pass through them. Tin oxide (SnO$_2$), ITO, fluorine doped tin oxide (FTO) and ZnO:Al are the most widely used materials. CdS is used as window layer in this type of cells, while CdTe is used as an absorber. Physical properties of materials used in CdTe based solar cells, and interface properties of CdS/CdTe solar cells are presented in Table 5.

Table 5 Important properties of CdTe based solar cell.

<table>
<thead>
<tr>
<th>Properties</th>
<th>Value</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TCO (SnO$_2$, ITO, FTO and ZnO:Al)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lattice constant SnO$_2$ (Å)</td>
<td>a=4.72; c=3.19</td>
<td>[629]</td>
</tr>
<tr>
<td>Lattice constant ITO (Å)</td>
<td>a=1.12</td>
<td>[630]</td>
</tr>
<tr>
<td>Lattice constant FTO (Å)</td>
<td>a=4.69; c=3.16</td>
<td>[631]</td>
</tr>
<tr>
<td>Lattice constant ZnO:Al (Å)</td>
<td>a=3.24; c=5.16-5.16</td>
<td>[632,633]</td>
</tr>
<tr>
<td>Work function SnO$_2$ (eV)</td>
<td>4.7-5.7</td>
<td>[634]</td>
</tr>
<tr>
<td>Work function ITO (eV)</td>
<td>4.7</td>
<td>[635]</td>
</tr>
<tr>
<td>Work function FTO (eV)</td>
<td>4.4</td>
<td>[636]</td>
</tr>
<tr>
<td>Work function ZnO:Al (eV)</td>
<td>3.83</td>
<td>[637]</td>
</tr>
<tr>
<td>TCOs Optical Transmission</td>
<td>&gt;80%</td>
<td>[638]</td>
</tr>
<tr>
<td>TCOs Resistivity $\rho$ (Ω·cm)</td>
<td>$10^{-4}$</td>
<td>[638]</td>
</tr>
<tr>
<td>Bandgap energy SnO$_2$ (eV)</td>
<td>3.9</td>
<td>[629]</td>
</tr>
<tr>
<td>Bandgap energy ITO (eV)</td>
<td>3.6</td>
<td>[639]</td>
</tr>
<tr>
<td>Bandgap energy FTO (eV)</td>
<td>3.3-3.6</td>
<td>[640,641]</td>
</tr>
<tr>
<td>Bandgap energy ZnO:Al (eV)</td>
<td>3.0-3.4</td>
<td>[642]</td>
</tr>
<tr>
<td><strong>Window layer (CdS)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lattice constant Cubic (Å)</td>
<td>a=5.83</td>
<td>[643]</td>
</tr>
<tr>
<td>Lattice constant Hexagonal (Å)</td>
<td>a= 4.14 c = 6.75</td>
<td>[644]</td>
</tr>
<tr>
<td>Work function (eV)</td>
<td>4.7</td>
<td>[645]</td>
</tr>
<tr>
<td>Bandgap energy (eV)</td>
<td>2.4</td>
<td>[627,639]</td>
</tr>
<tr>
<td><strong>Absorber layer (CdTe)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lattice constant (Å)</td>
<td>a=6.48</td>
<td>[646]</td>
</tr>
<tr>
<td>Work function (eV)</td>
<td>3.88-4.09</td>
<td>[647]</td>
</tr>
<tr>
<td>Enthalpy of formation (J/mol)</td>
<td>$10^6$</td>
<td>[648]</td>
</tr>
<tr>
<td>Standard entropy (J/mol.K)</td>
<td>-4.3±0.8</td>
<td>[648]</td>
</tr>
</tbody>
</table>
Carrier concentration/cm³ (p-type CdTe) | $10^{14}$ | [625, 649,650]
Lifetime electron/holes $\tau$ (s) 2µm | $10^{-9}$ | [626]
Bandgap energy (eV) | 1.45 | [639]

**Interface (CdS/CdTe)**

| Mistmatch cubic CdTe and hexagonal CdS | 9.7% | [651, 652]
| Mistmatch cubic CdTe and cubic CdS | - | -
| CdTe Absorption co-efficient/cm (at ~600nm) | $>10^5$ | [625, 626, 653]
| Dielectric constant CdS/CdTe ($\varepsilon/\varepsilon_o$) | 10/9.4 | [639]
| Electron mobility $\mu_e$ CdS/CdTe (cm²/Vs) | 350/500-1100 | [639, 654]
| Hole mobility $\mu_h$ CdS/CdTe (cm²/Vs) | 50/60-100 | [639, 654]
| Minority-carrier diffusion length (µm) | <0.8 | [625]
| Capture cross section electrons $\sigma_e$ CdS/CdTe (cm²) | $10^{-17}/10^{-12}$ | [639]
| Capture cross section holes $\sigma_h$ CdS/CdTe (cm²) | $10^{-12}/10^{-15}$ | [639]

From crystallographic point of view, the lattice mismatch and crystallographic structure among all components that form the solar cell heterostructure are of essential importance. Figure 75 shows the crystallographic structure of both CdTe and CdS layers in the cubic zincblende (Fig.75a) and hexagonal Wurtzite structure (Fig.75b).

Fig. 75 Crystallographic structure of (a) zincblende, and (b) hexagonal Wurtzite. In the zincblende structure, tellurium or sulphur atoms occupy the tetrahedral position surrounded by cadmium atoms located in a face-centered cubic structure. While in the Wurtzite structure, tetrahedron is formed when the S atom is in the interior of the hexagonal structure. CRYSTALMAKER program is used to create the structure even though this is a well known structure.

### 9.2 Thin-film CdS/CdTe solar cells

In general, the transport of the photogenerated minority-carriers in bulk thin film materials and single crystals has the advantage of fast transportation due to low number of
defects. At the same time there is a disadvantage that the production methods require high energy consumption at high cost and large mass of initial starting materials. The fabrication of CdS/CdTe solar cell has been mainly carried out using chemical bath deposition (CBD), sputtering and evaporation, close space sublimation (CSS), and MOCVD [627].

9.2.1 Concepts and preparation methods

P-type CdTe possesses an optimum direct bandgap (1.45eV) and high optical absorption co-efficient ($5 \times 10^5/\text{cm}$) in the visible spectral range. A 0.5 $\mu$m thick CdTe is able to absorb a large percentage (99%) of the solar spectrum [625,652,655]. To form heterojunction, n-type CdS between 10 and 50 nm layer is required to minimize the photon absorption losses, without reducing the $V_{oc}$ [652]. Currently work is being carried out in order to improve the window layer.

For CdS/CdTe solar cells, superstrate configuration is the most commonly used with the structure illustrated in Fig. 74 [625,656]. Substrate configuration with low-cost flexible metal substrate is also used [657]. In these configurations, most of the efforts are concentrated on improving the quality of both window and absorber layers. This is along with reducing losses through the other components and interfaces due to light absorption in layers other than the CdTe. Developing a successful solar cell requires a combination of improving the quality of all components including the electrodes, enhancement of charge transport, and hence cell efficiency [30].

For the preparation of CdS layer by CBD method, a mixture of KOH, ammonium nitrate, CdCl$_2$, and thiourea are generally used at a working pH value of 8-9 in the temperature range of 75-90°C. A magnetic stirrer in the solution is used to maintain a homogenous solution and to control the thickness of the CdS film. In order to obtain the required thickness, the most important parameters in the growth process are pH, temperature, stirring rate, and time [658, 659].
CSS method is a physical deposition technique where the source and the substrate are very close to each other, thus allowing the sublimation of the source and creating epitaxial thin films without using ultra high vacuum. Using this technique both the window and the absorber layers are prepared [625, 651, 655, 660-662]; the most sophisticated CSS system are located in the Technical University of Darmstadt (with in situ characterization tools for a complete study of the solar cell) [656, 662], and CTF Solar GmbH [663]. Figure 76 shows the schematic diagram of a CSS system for the deposition and processing of CdS and CdTe layers. A general approach for the CSS method [649, 656, 662, 663] uses commercial halogen lamps for heating the source and substrate. As an alternative to halogen lamp, resistance heaters (SiC) have been recently proposed as an approach to reduce the duration of the process and improving the grain size and homogeneity [664]. Several deposition parameters must be taken into account, such as controlled high-vacuum or inert atmosphere, source temperature in the range of 500-650°C, substrate temperature in the range of 300-500°C, distance between source and substrate of 2-5mm, and deposition time of 5-20 min. A fast (1 min) or slow (15 min) cooling process after the CdTe layer preparation in the 300-500°C range has been considered as an important step with great influence in the absorber layer preparation, with fast cooling yielding slightly thicker Cd layer. This thick Cd-layer could influence the CdCl₂ diffusion [649] and affect efficiency.
Fig. 76 Schematic diagram of close space sublimation system for the preparation of CdS and CdTe films [665].

Distance between the source and substrate is 2-5mm and the deposition time is around 5-20min. In order to reduce the contamination between three sources, a precise shutter is located over each source, and a vacuum process is done before CdS layer deposition. Source temperature and substrate temperature is in the range of 500-650°C, and 300-500°C respectively. The top substrate is located in a moveable piece over fixed sources with the capability for depositing several consecutive different layers of CdS, and CdTe. At the same time, cadmium chloride (CdCl₂) treatment could be carried out in the same system. After each layer deposition, CdCl₂ treatment is required to improve electronic properties.

For CdS/CdTe cell fabrication, there is a general agreement that after the deposition of each layer (CdS and CdTe), CdCl₂ treatment is necessary to improve electronic properties, recrystallization, grain growth [666] and hence cell efficiency. Prior to CdCl₂ treatment, Major et al. [649] showed the importance of creating (tens of nanometers thick) Cd-rich surface using nitric-phosphoric acid etching to increase the chlorine and oxygen in-diffusion associated with an improvement in the efficiency from <3% to 12%. The absence of this etching process will, however, produce a blocking layer of Cd₃O₂Cl₂.

For CdS layers, CdCl₂ treatment is used because of the resulting benefits of the window layer causing a recrystallization and increasing the grain size with improvement of the structural and optoelectronic properties [625,661, 662-665, 667].

For CdTe layers, post treatment with a CdCl₂ treatment is generally used as a process to promote the interdiffusion of CdS/CdTe layer and recrystallization. The result is the improvement of the texture and grain size, and reduction of porosity, with reduction of the
point defects [625, 657, 662]. However, CdTe surface roughness increases after CdCl₂ treatment [666]. At the same time, the introduction of chlorine can compensate native defects in the CdTe structure [668]. In the end, this post treatment affects the interdiffusion at the CdTe/CdS interface with the consequence of reducing the negative factor of the large mismatch between both materials [651, 652, 655].

Other important layers to be considered are the front and back contact, where some novelties have been reported. For the front contact, the ZnO:Al is increasingly used, although their lower thermal stability has many advantages compared to other (ITO, FTO) front contact materials [642, 662]. For the back contact, a 4-5nm Cu, followed by a 40-100nm gold (Au) layer, is the most used. The Au layer is replaced by antimony telluride to avoid the Cu diffusion towards the interface [650, 662, 663, 669]. In a complementary way, the use of selective acidic etching for a formation of tellurium or a p⁺-layer prior to the contact formation is an interesting process, which will improve the back contact [647, 662].

### 9.2.2 CdTe solar cell parameters and properties

Table 6 shows CdTe solar cell parameters. It can be seen that the device with maximum efficiency of 19% has the best \( V_{oc} \) and \( J_{sc} \) values [670]. Figure 77 shows the efficiency versus \( V_{oc} \) values, where a clear dependence among both values is demonstrated.
Fig. 77 Relationship between $V_{oc}$ and efficiency. The data corresponds to the values shown in Table 6. As can be seen, there is a direct relationship between $V_{oc}$ and efficiency. Efficiency >14% has been obtained when $V_{oc}$ is greater than 750mV. To obtain high $V_{oc}$ and $J_{sc}$, CdTe thickness of 2-5µm is required.

Table 6 CdS/CdTe solar cell output parameters.

<table>
<thead>
<tr>
<th>Institution</th>
<th>$V_{oc}$ (mV)</th>
<th>$J_{sc}$ (mA/cm²)</th>
<th>Fill factor (%)</th>
<th>Eff. (%)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>University of Liverpool</td>
<td>635</td>
<td>20.2</td>
<td>47.1</td>
<td>8</td>
<td>[671]</td>
</tr>
<tr>
<td>Darmstadt University of Technology</td>
<td>775</td>
<td>23.9</td>
<td>64.9</td>
<td>12</td>
<td>[662]</td>
</tr>
<tr>
<td>University of Chicago</td>
<td>684</td>
<td>25.8</td>
<td>71</td>
<td>12.3</td>
<td>[641]</td>
</tr>
<tr>
<td>CTF Solar GmbH</td>
<td>838</td>
<td>21.8</td>
<td>71.1</td>
<td>13</td>
<td>[663]</td>
</tr>
<tr>
<td>University of Oregon</td>
<td>790-840</td>
<td>23.0-24.4</td>
<td>62-72</td>
<td>11-14</td>
<td>[668]</td>
</tr>
<tr>
<td>University of Toledo</td>
<td>806</td>
<td>25.2</td>
<td>69.8</td>
<td>14.2</td>
<td>[669]</td>
</tr>
<tr>
<td>University of Toledo</td>
<td>847</td>
<td>24.4</td>
<td>69.8</td>
<td>14.5</td>
<td>[672]</td>
</tr>
<tr>
<td>University of Durham</td>
<td>840</td>
<td>24</td>
<td>73.41</td>
<td>14.8</td>
<td>[649]</td>
</tr>
<tr>
<td>Ferdowsi University of Mashhad</td>
<td>860</td>
<td>25.7</td>
<td>81.8</td>
<td>18.1</td>
<td>[639]</td>
</tr>
<tr>
<td>First Solar, Inc</td>
<td>872</td>
<td>28</td>
<td>78</td>
<td>19</td>
<td>[670]</td>
</tr>
<tr>
<td>First Solar, Inc</td>
<td>875</td>
<td>30.2</td>
<td>79.4</td>
<td>21</td>
<td>[484]</td>
</tr>
</tbody>
</table>

The dependence of $V_{oc}$ and $J_{sc}$ on CdTe layer has been studied extensively [626, 646, 654]. For CdTe, absorption in the solar spectrum is ~93% for 1µm thickness, while 99% absorption requires ~20µm thickness. For 1µm thickness, $J_{sc}$ decreases more than 20% with strong interdiffusion effects on the CdS/CdTe layer, while it decreases only ~5% for 2-3 µm [654]. For this reason, in order to obtain an optimum value of $V_{oc}$ and $J_{sc}$, a critical thickness of 2-5µm may be required [652, 654, 657, 663].

9.2.3 Defects in CdTe solar cells

Defects such as dislocations, traps, and grain boundaries are important factors that affect efficiency in planar CdTe solar cells. For this reason, defects have been investigated experimentally, as well as theoretically in order to study the influence of these on the optoelectronic properties and consequently on the solar cell efficiency. The quality
improvement for each component, viz. front contact, window layer, absorber layer and back contact is essential to increase cell performance. The following improve device performance:

(i) A good texture of TCO layer will enhance orientation of CdS film.

(ii) Pin hole free CdS window layer is essential to reduce losses that are associated with recombination at interfaces. CdS layer thickness below 80 nm could produce pinholes and increase shunting effects [627,656].

(iii) The presence of grain boundaries affect preferential interdiffusion of sulfur (S) from CdS to CdTe as a consequence of assisted diffusion mechanism leading to the formation of the CdTe_{1-x}S_x phase. Grain boundaries induce dislocations, trap minority carriers, and influence V_Oc [653] which reduces cell efficiency. At the same time the internal electric field that exists between the grain boundary core and the bulk material will deteriorate the electrical conductivity of the material [653, 673].

(iv) CdTe layer requires a thickness of 3-5μm to avoid pinholes and shunting phenomena. Therefore, a double CdTe layer structure formation has been prepared with two consecutive temperature steps [650].

(v) All interfaces must be carefully controlled. In fact, distorted bonds at the interfaces introduce extra electronic states, hole traps, and accumulation of positive charges [653].

9.2.4 Novelties and improvements

For the development of planar CdS/CdTe solar cells some general novelties have been proposed:

(i) With spin coating process, tens of sequentially controlled thickness layers can be produced [641].

(ii) The use of nanoparticles as source material in CSS method will reduce the time for obtaining a pre-determined thickness of the CdTe layers. As one example, for a given 5μm thickness, a reduced time of 35% is obtained [641].
(iii) In CSS high vacuum process, a double layer structure formation with two consecutive temperature steps for both window and absorber layer is suggested in Ref. [650].

The new features and improvements that have been introduced recently in the development of CdS and CdTe layers as well as developments in the characterization techniques are described below:

(i) An extra oxide layer between the TCO and the window layer to minimize shunting effects has been introduced. However, it also comes with the disadvantage of increasing production cost [627]. In fact a ZnO buffer layer before the CdS window layer has been proposed as a factor for reducing pinholes and voids on the window layer [657].

(ii) CdS window layer prepared with low oxygen content in the order of 2% O₂/Ar gives a good adhesion layer after CdCl₂ treatment, while without O₂ treatment, the interface is delaminate [674]. At the same time, the O₂ partial pressure will enhance the transmission below 500nm with slightly increase in efficiency of 1% [674].

(iii) Widening CdS layer bandgap to allow more region of the solar spectrum to reach the absorber layer with improving photocurrent. For example Cd₁₋ₓZnₓS composition enhances the blue-region of solar spectrum with increasing Zn concentration being the bandgap energy values 2.4-3.5 eV for Cd₁₋ₓZnₓS (0<x<0.9) [627]; Also, smoother and denser CdS layers have been proposed as a measure to reduce the light absorption in the high energy UV range [627, 656].

(iv) The doping of p-type CdTe layer has been proposed as a way to modify carrier recombination and increase the shallow acceptors in p-type CdTe to improve bulk minority-carrier lifetime [625]. It is also a way to increase the work function with dopants such as arsenic, although arsenic segregation at the grain boundaries will increase the acceptor concentration in these regions [647]. Furthermore, a step doping profile of the absorber layer has been done with a structure of p/p+ with thickness ratio of 2.24/1.26μm as a way to create...
an electric field that improves carrier collection [639], resulting in an improvement in $V_{oc}$, improved fill factor, efficiency, and reduction of the series resistance [639].

(v) Large difference in the valence band offset at the interface will form a barrier for holes, with an increase in the contact resistance. To obtain negligible valance band offset for efficiency enhancement, wide bandgap materials such as Cd$_{1-x}$Zn$_x$Te ($E_g \sim 1.5-2.4$eV), Cd$_{1-x}$Mn$_x$Te ($E_g \sim 1.5-3.2$eV) and Cd$_{1-x}$Mg$_x$Te ($E_g \sim 1.5-3.6$eV) are used with appropriate composition ratios of Zn, manganese (Mn) and magnesium (Mg), all of them having high solubility in CdTe [625,626].

(vi) For absorption of low energy photons, an intermediate narrow metallic bandgap material is used between the n/p type semiconductors [30].

(vii) In the absorber/contact interface, the use of electron reflector barriers such as CdXTe (X:Mn, Zn, Mg) are useful for reducing back surface recombination, which allows increased values of 0.2V for $V_{oc}$ and 3% for the efficiency. This is a strategy used for CIGS and Si-based solar cells, although here the quality of the interface between absorber/electron barrier must be improved [626]. The other way of increasing efficiency is the use of highly doped ($10^{18}$/cm$^3$) buffer layer at the interface between absorber/contact in the substrate configuration [657].

Apart from classical techniques such as XRD, scanning electron microscope (SEM), EDX etc. it is of special interest to know new tools that have been successfully used in the past few years for better understanding the properties of CdTe solar cell. These include scanning Kelvin probe microscopy for the Fermi level shift determination and CdTe work function [647], laser beam induced current for photoelectronic properties [653], electron beam induced current [664] and electron back-scatter diffraction to demonstrate that the grain structure and the grain boundaries dominate the electrical activity [673], x-ray photoelectron spectrometer for in situ measurements in the CSS chamber [656], thermo photocurrent
measurements to investigate the compensating levels introduced by CdCl₂ treatment [668] etc.

9.3 CdTe nanostructured solar cells

Extensive research has been carried out in the field of 3G solar cells over the past several years [623, 628, 635, 657, 667, 675-684]. The basic structure of these nanostructured solar cells follows the general configuration of the planar solar cells, where the front and back contacts, window layers, and absorber layers must be present. In this general configuration of the solar cell, nanostructures can be incorporated through top-down and bottom-up processes. Top-down processes such as the lithography, low energy ion sputtering [675], and laser irradiation [684] can change the solar cell properties, producing an improvement in luminescence and the crystallinity.

Due to a large number of possibilities, this section will focus on the bottom-up structures where the nanostructures are created as an intermediate step in the fabrication of solar cell, and on the superstrate configuration.

Excellent reviews have been published [671, 685] about the new perspectives of the enhancement of the solar cells efficiencies with the use of 1D nanostructures, nanopatterning and their applications, in particular dye/quantum dots sensitized solar cells, and single/double wall carbon nanotubes as strategies for new nanostructured architecture of inorganic and organic solar cells. This new technology is being used in CdS/CdTe solar cells.

9.3.1 Concepts and advantages

The concept of nanostructure on CdTe solar cell, requires a general configuration of a superstrate structure (glass/TCO/CdS/CdTe/back contact), with the presence of nanostructures in some of the layers. These nanostructures play an important role with promising properties in metals, oxides, semiconductors, etc. having an extraordinary
importance in PV energy production due to the decoupling of light absorption and carrier separation into orthogonal special directions [676].

The concept and structure of nanostructures embedded in bulk film indicates that the longitudinal direction is long, allowing for optimal and enhanced light absorption due to more internal reflections and longer path length compared with thin-films, while the orthogonal direction is thin allowing for an effective minority-carrier collection [676]. The size and spacing are in the order of the light wavelength, resulting in positive anti-reflective and light trapping properties, with a reduction of the reflectance of two orders of magnitude compared to the equivalent planar structures. This allows for a high performance without a reduction of the $J_{sc}$ [657, 676].

In the nanostructured solar cell, apart from lower defect trapping, the diffusion length of minority-carriers in the lateral direction is shorter than that of a thin-film solar cell [686]. Nanojunctions generate an electric field in the lateral direction that gives the option to the minority-carrier to move between the core and the shell, resulting in relatively short carrier transit length, and consequently the recombination loss is reduced [657,687]. Broadening of the optical bandgap with the use of nanostructure could maximize the S-Q efficiency limit which is an attractive electronic property.

9.3.2 Types of nanostructures and mechanisms of formation

There are different types of nanostructures that follow the general scheme of a core structure of ZnO or CdS embedded by the shell structure of CdS or CdTe respectively, named as ZnO/CdS [681, 683] or CdS/CdTe core/shell structure [677, 685], although there are some exceptions to this rule. As mentioned in Sec. 7.6.1, the nanostructures can be classified according to their structure as follows: nanowires [677, 681, 683, 685], nanocones [676, 684, 686], nanopillars [685] and whiskers or needles [677].
There are several methods for core formation. The most general processes use Au and Ni as catalyst for nanowire core formation through the VLS process [16, 657, 677, 680, 687]. Nevertheless, there are other methods used for core formation: porous anodic alumina substrates embedded in polycrystalline thin-films for p-type CdTe formation [685], patterned nanoelectrodes defined on the TCO substrate through e-beam lithography with hole size of 0.4-1nm [688], and magnetron sputtering deposition using Ar [678].

For core/shell formation, the core begins from a seed material where nanowire crystallizes or grows, as it happens with Au catalyst. Other methods are: a µm layer of CdTe as a seed for the growth of CdTe nanowire in substrate configuration [657]; a nm thick ZnO:Al buffer layer on ITO substrate and using CVD process to develop nanocones shaped ZnO [686]; TiO₂ nanoparticles deposited by dip-coating on FTO substrate for the preparation of ZnO nanowire by chemical solution, followed by the growth of nanotubes of CdS in a chemical galvanostatic process [679]; another alternative for the ZnO nanowire is the previous creation of ZnO seed layer, with the added advantage that this layer could avoid shunting paths [681, 683, 686].

The other alternatives that may be of high interest for CdTe nanostructured solar cell are: the use of nanoink solution processes containing organic ligands and applied in ambient conditions as a way for nanolayer formation [623]; the use of graphene monolayer with conductive polymer interlayers, and a spin coating of zinc layer as a mean for ZnO nanowire preparation in aqueous solutions at a relatively low-temperature [682].

The growth mechanism of CdTe nanowire solar cell has been rarely studied. Nevertheless, Ref. [678] demonstrates that the CdTe nanowire formation follows the Stranski-Krastanov model determined by the free energy of the substrate surface ($\sigma_s$), interface free energy ($\sigma_i$) and heteroepitaxial surface free energy ($\sigma_f$). In consequence, the seed crystal is nucleated in the 2D layer when $\sigma_s$ is larger than the addition of the other two,
and 3D islands are formed when $\sigma_s$ is smaller than the addition of the other two. The growth process is controlled by the concentration of the nanowire and depends on the temperature and the type of substrate used.

Growth process indicates that growth rates up to $1\mu$m could be obtained due to solid and vapor phase growth mechanism [657]. A preferential orientation of $<111>$ in CdTe film over the ZnO nanowires, with the appearance of side wall facets has been reported [657, 686]. An interesting sulfidation process has been proposed using the following route: ZnO nanowire produced through a chemical solution is followed by sulfidation (with thioacetamine) of the ZnO nanowire for the production of ZnO/ZnS core/shell structure, and completed by the ion exchange Zn-Cd with the result of ZnO/CdS core/shell nanowire structure. This is due to the fact that the solubility product of CdS is $10^4$ times lower than ZnS [683]. Also, nanowire heterostructures on III-V Wurtzite/zin-blende cubic compounds [680] with similar crystallography structures of CdS/CdTe have been studied, and a growth mechanism is explained through the competition between the Gibbs-Thomson effect and the different diffusion mechanisms.

The post growth process that follows the nanostructure formation is similar to that of planar solar cell. To improve efficiency, CdCl$_2$ treatment in one or several steps is essential for recrystallization controlling the interdiffusion at the CdS/CdTe interfaces and passivation of the grain boundary interfaces [657, 667, 686, 689].

9.3.3 Characteristics of nanostructures and CdTe nanostructured solar cells

Table 7 shows the most important characteristics of the nanostructures used in CdTe solar cells, with indication of the preparation methods and nanowire characteristics such as diameter, height, density, and spacing between the nanowires. There are different methods from chemical solution to vapor, which produce nanowire geometries with clear difference
between them. Considering the three nanowires geometric properties of diameter, height and density, if one considers that the ratio between height and diameter is critical for efficiency, a general conclusion to draw is that the VLS method is the most adequate for nanowire formation. In the spacing data, there are differences between the reported values that appear to be related to preparation method.

Table 7 Characteristics of the CdTe Nanostructures.

<table>
<thead>
<tr>
<th>Nanowire Structure</th>
<th>Method</th>
<th>Diameter (nm)</th>
<th>Height (µm)</th>
<th>Density (/cm²)</th>
<th>Spacing (nm)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZnO</td>
<td>CBD</td>
<td>140</td>
<td>5</td>
<td></td>
<td>0.3</td>
<td>[681]</td>
</tr>
<tr>
<td>ZnO</td>
<td>CVD</td>
<td>80-300</td>
<td>1</td>
<td>$10^9$</td>
<td>20-200</td>
<td>[686]</td>
</tr>
<tr>
<td>ZnO</td>
<td>Dip-coating</td>
<td>80</td>
<td>1</td>
<td>$10^{10}$</td>
<td>20-40</td>
<td>[679]</td>
</tr>
<tr>
<td>CdS</td>
<td>PLD</td>
<td>40-100</td>
<td>0.4-1</td>
<td>$2\cdot10^9$</td>
<td></td>
<td>[677]</td>
</tr>
<tr>
<td>CdS</td>
<td>Electro-deposition</td>
<td>60</td>
<td>100</td>
<td>$1.14\times10^{10}$</td>
<td>106</td>
<td>[627]</td>
</tr>
<tr>
<td>CdTe</td>
<td>VLS</td>
<td>50-200</td>
<td>10-100</td>
<td>$10^7-10^8$</td>
<td></td>
<td>[657]</td>
</tr>
<tr>
<td>CdTe</td>
<td>Sputtering</td>
<td>100-150</td>
<td>3</td>
<td>$\sim10^9$</td>
<td>20-50</td>
<td>[678]</td>
</tr>
<tr>
<td>CdTe</td>
<td>Electro-deposition</td>
<td>400-1000</td>
<td>1</td>
<td>$\sim5\times10^9$</td>
<td>2000</td>
<td>[688]</td>
</tr>
</tbody>
</table>

The output characteristics of the CdTe nanostructured solar cells are indicated in Table 11.8, where the relatively low efficiency can be observed if one compares these data with planar solar cell, although the improvement has been steadily increasing over the years. An example of this increment is a new efficiency record for this type of devices of 12% using CdS nanowires embedded in CdTe [628], with a high value of $J_{sc}$ (26mA/cm²).

Table 11.8 Output characteristics of nanostructured CdTe solar cells under AM 1.5 conditions.

<table>
<thead>
<tr>
<th>Institution</th>
<th>$V_{oc}$ (mV)</th>
<th>$J_{sc}$ (mA/cm²)</th>
<th>Fill factor (%)</th>
<th>Eff. (%)</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oak Ridge National Laboratory</td>
<td>630</td>
<td>8.3</td>
<td>38</td>
<td>2</td>
<td>[686]</td>
</tr>
<tr>
<td>University of Liverpool</td>
<td>520</td>
<td>13.9</td>
<td>34.3</td>
<td>2.49</td>
<td>[657]</td>
</tr>
<tr>
<td>Oak Ridge National Laboratory</td>
<td>610</td>
<td>13.8</td>
<td>38</td>
<td>3.10</td>
<td>[686]</td>
</tr>
<tr>
<td>University of Kentucky</td>
<td>770</td>
<td>26</td>
<td>60</td>
<td>12</td>
<td>[628]</td>
</tr>
</tbody>
</table>
Future direction

More work and investment must be done considering the predicted maximum theoretical efficiency of 29%. Here are some research paths that could be followed to improve the efficiency: (i) improvements in front contacts by replacing TCO by graphene, pure and doped, together with buffer layers allowing for Ohmic contacts [682, 690], (ii) well aligned CdTe nanowires with optimum value of the diameter/thickness ratio, (iii) strategic alloys and compounds to increase the bandgap of the buffer layer for improving efficiency, and (iv) adequate buffer layers for lattice mismatch reduction in order to improve the crystallographic quality.

SiNW solar cells

With the beginning of this millennium it was rapidly realized that nanostructures such as SiNWs offer a flexible platform for novel 3D solar cell concepts [691-693]. Nanowires show several advantages over planar solar cell geometries such as the potential for increased device density, and device development on flexible substrates. Direct bandgaps in smaller diameter SiNWs also offer the potential for increased efficiency. Since Si is well understood in terms of its properties, SiNWs come with a solid platform for extending current fabrication technology in their use as active solar cell materials.

This section will give a short overview about SiNW based solar cells, present the competing concepts and show the most promising candidates for highly efficient and cost-effective solar cells.

The term nanowire is often substituted by related terms like nano-rods, whiskers, pillars, columns or cones. A recent review by Kuang et al. therefore formed the description “elongated nanostructures” to combine all these different terms with a similar meaning [694].

SiNW formation
SiNWs can be prepared by several different techniques and every method has its own advantages and drawbacks. The large increase in surface area enables an efficient light trapping due to multiple scattering events and optical path increase inside the SiNW. In general, the nanowire synthesis methods are arranged in bottom-up growth and top-down etching techniques.

In the case of bottom-up synthesis, the VLS growth, which was developed by Wagner & Ellis in 1964, is the most popular approach of preparation [695]. As mentioned in Sec.7.6.1, in a VLS process, a metal catalyst which forms a eutectic with Si (Au, Al, Cu and Ag etc.) is heated in vacuum and is exposed to a gaseous Si source like SiH₄, tetrachlorosilane (SiCl₄), sputtered or laser ablated Si [696-699]. Most research groups used SiH₄ precursors for SiNW growth since it can produce well controlled wire dimensions and is relatively easy to handle once the toxicity is kept under control. A VLS process requires a high or ultrahigh vacuum chamber in which a substrate covered with the catalyst metal, in the form of particles or a thin-film, is heated above the eutectic temperature. The SiH₄ molecules are decomposed on the metal surface and the Si is introduced into the metal droplet, forming the eutectic. By further insertion of Si, the droplet gets oversaturated and excess Si is displaced to the contact surface of the droplet to the substrate. In this way a wire arises below the droplet. By controlling the catalyst geometry, chemistry and process parameters, it is possible to create nanowires with precise lengths, diameter, direction, doping and pitch. The advantage of high control has to be weighed by the disadvantages of high costs for vacuum equipment, highly poisonous gases and catalyst metal contamination inside the wires, which is the major drawback especially for Au catalyzed SiNWs [700].

Nevertheless, there are many groups that successfully created solar cells out of VLS-grown SiNWs. Hochbaum et al. showed the advantages of using SiCl₄ as a precursor [701]. During the decomposition of the precursor molecules HCl vapor is formed which etches and
thus cleans both the SiNW sidewalls as well as the substrate surface. In this way it became possible to grow highly ordered epitaxial SiNWs, which was not possible with SiH₄. The electrical modification of SiNWs is achieved by adding doping precursors like B₂H₆ or PH₃ into the chamber during growth which leads to p- or n-type doping [692,702] respectively. In 2006, Wang et al. described the growth of SiNWs by using Al catalyst to avoid the deep-level electronic states that are caused inside the Si when using a gold catalyst [698]. On the other hand Al comes with another drawback: it needs an extremely clean environment at UHV conditions to avoid oxidation of the Al which drives the production costs to a disproportionate level.

Garnett & Yang [532] and Stelzner et al. [703] developed the first solar cell devices based on carpets of SiNWs grown by VLS method. Their efficiencies were quite low, but they established a basis for a complete new field of nanostructured solar cells.

In contrast to the bottom-up growth methods, the top-down synthesis of SiNWs uses existing layer of Si like single- or multicrystalline wafers or deposited layers on supporting substrates to create wires inside these layers. The most prominent processes are the metal-catalyzed electroless etching, which was developed by Peng et al. [693] in 2002, and the RIE [704,705]. Both processes can form randomly distributed or ordered SiNWs.

In a metal-catalyzed electroless etching (MCEE) preparation, a metal catalyzed anisotropic etching of Si forms the desired SiNWs. The most prominent recipe was developed by Peng et al. [693,706]. Ag nanoparticles are deposited on Si in a mixture of HF/silver nitrate and are subsequently used for the anisotropic etching in a HF/H₂O₂ mixture. The Si is catalytically oxidized at the Si/metal interface and immediately etched by the HF. In this way, the metal particles move into the Si layer, forming a carpet of SiNWs. Since the anisotropic etching at room temperature only occurs in the Si<100> direction [707], perpendicular SiNWs are formed on a Si(100) wafer (Fig. 78), while the use of a Si <111> wafer leads to
zig-zag shaped wires [708]. In multicrystalline layers, each grain is independently etched into the <100> direction [709]. MCEE processes are easily scalable and relatively cheap in contrast to bottom-up growth which is why it is an attractive way of generating highly absorbing structures for photovoltaics.

Fig. 78 Left side: Schematic model of the preparation of wet-chemically etched SiNWs. Ag nanoparticles are deposited by rinsing a wafer in a silver nitrate/HF mixture. These particles act as catalysts in the subsequent etching of Si in HF/hydrogen peroxide which is highly dependent on the crystal orientation of the wafer. In the final step Ag is removed by nitric acid. Right side: A tilted (55°), colored SEM micrograph of an etched Si<100> wafer with SiNW length of 2µm. Such a structure acts as a nearly perfect light absorber with an absorption of over 90% in a wavelength range from 400 – 1000nm. SEM image originally published in [710], Björn Hoffmann, Vladimir Sivakov, Sebastian W. Schmitt, Muhammad Y. Bashouti, Michael Latzel, Jiří Dluhoš, Jaroslav Jiruse and Silke Christiansen, "Wet–Chemically Etched Silicon Nanowire Solar Cells: Fabrication and Advanced Characterization in Nanowires"- Recent Advances., InTech; 2012. Edited by Xihong Peng. pp-211-230. Reproduced here under CC BY 3.0 license. Copyright © 2012 InTech.

In addition to wet-chemical processes there is much effort put into the development of dry-etching of Si in a deep RIE (DRIE) approach. The process works without metal catalysts and can be applied either in a self-organized or a mask-supported process. Two particular approaches will be mentioned here: the formation of so-called black Si and the preparation of highly regular SiNWs by the use of nanosphere lithography. The term black Si is used for many variations of etched Si and refers to the dark appearance of such a layer. In the most popular results, a fluorine-based etching [711-713 827-829] creates random pyramidal or needle-like structures that can be compared to MCEE results. The advantage is that no lithography step for catalysts or masks is needed. Halbwax et al. used a femtosecond laser to form Si nanostructures that also carry the name black Si [714].
By combining a RIE process with a prior decoration with a monolayer of silica spheres in a Langmuir-Blodgett deposition, Hsu et al. gained a high control over the dimensions of the resulting nanostructured Si [705]. Since the RIE approach produces SiNWs with a high dimensional reproducibility, which offers a precise tailoring of optical properties, it is one of the most promising fabrication mechanisms at the moment. Garnett & Yang have investigated the light trapping properties of RIE-prepared SiNWs in c-Si wafers and found an increase in path length of incident light inside the SiNW layer by a factor of 73 [715]. In 2012, Schmitt et al. have shown that such a combination of nanosphere lithography and RIE also produces regular vertical SiNWs in multicrystalline Si layers on glass and that the SiNW orientation is not influenced by the original grain orientations [716]. Figure 79 shows SEM micrographs and electron backscatter diffraction investigations of such prepared SiNWs. Since this process is more complicated and expensive, it is mostly used for fundamental research of optical properties or comparisons with theoretical models. Nevertheless, impressive results have been obtained with RIE prepared SiNWs and the current progress is very promising.

![SEM and electron backscatter diffraction mappings of multicrystalline thin-film Si that was patterned with regular SiNWs. This figure shows that the reactive ion etching doesn’t interfere with the crystal orientation of the substrate. All wires are perpendicular to the surface. Furthermore, even wires with a grain boundary inside them remain in a regular shape. Reprinted with permission from [716], Sebastian W. Schmitt, Florian Schechtel, Daniel Amkreutz, Muhammad Bashouti, Sanjay K. Srivastava, Björn Hoffmann, Christel Dieker, Erdmann Spiecker, Bernd Rech, and Silke H. Christiansen, Nanowire Arrays in Multicrystalline Si Thin Films on Glass: A Promising Material for Research and Applications in Nanotechnology, Nano Lett., 12 (2012) 4050. Copyright © 2012 American Chemical Society. Permission granted.](image-url)
10.2 Nanowire solar cell concepts

SiNWs open up new prospects in fundamental research and applications. Lieber and co-workers created the first reported single nanowire solar cells in axial [717] and radial [718] geometry and reached efficiencies of 3.4% in the case of radial/coaxial cells and 0.5% in case of the axial geometry. These fundamental studies showed the potential and limitations of nanowire-based solar cells and influenced the whole research community since then.

In this review we focus more on realistic applications and industry relevant realizations of nanowire solar cells. Therefore we will present several different concepts of radial or axial geometries, bulk or thin-film based SiNWs and random or organized SiNW-based solar cells. In general, nearly all concepts that are realized in planar geometries, which were already presented in this article, can be transferred to nanowire-based solar cells.

10.2.1 Axial and radial junctions

Nearly all SiNW solar cell concepts with a reasonable efficiency or a promising geometry are based on radial junctions instead of axial junctions, since one of the major advantages in a radial concept is the decoupling of absorption path and charge carrier separation path. Nevertheless, there are several realizations of axial solar cells reported. In 2004 Peng et al. fabricated p-n junctions along SiNW carpets by using MCEE on planar p-n junction wafers [719]. Even though the realized junctions were not suitable for solar cells, Sivakov et al. were able to use a similar preparation on multicrystalline Si thin-films on glass to form axial p⁺-n-n⁺ junctions which showed a conversion efficiency of 4.4% [709].

A radial junction geometry is more and more preferred for SiNW-based solar cells in the last years. In 2005, Kayes, Atwater and Lewis published a theoretical modelling of radial p-n junctions in Si nanorods and the model showed that a large increase in efficiency is possible compared to planar p-n junctions [720]. The calculations also showed the crucial points that had to be concerned: low minority-carrier diffusion lengths compared to the
optical thickness and low depletion region recombination. This concept shows the potential of utilization of lower quality Si materials and cost reduction towards a possible mass production.

In the early days (2007-2008) of radial SiNW solar cell development mostly VLS grown SiNWs were used [535,703], but the efficiency only reached very low values of 0.1%. Nevertheless, these initial studies found the crucial points which have to be optimized, like the contamination with catalyst atoms or the junction quality. Recently, VLS grown SiNWs undergo a renaissance, as Cho et al. prepared SiNWs with Sn as a catalyst and reached nearly 5% efficiency [721]. Their concept uses a crystalline p-type Si core with intrinsic and n-type a-Si:H shells grown on ZnO:Al covered glass, as shown in Fig. 80. One year later in 2013, the same group improved their cell concept to an excellent efficiency of 8.14% by optimizing the nanowire density [722].

Fig. 80 (a) Schematic of a p-c-Si/i-a-Si:H/n-a-Si:H junction geometry on glass substrate. The SiNWs are grown on ZnO covered glass and both SiNWs and substrate are subsequently covered by an intrinsic and an n-type a-Si.
In terms of scalability, and thus industry relevance, top-down prepared SiNWs play a more important role. In 2010, Garnett and Yang presented radial p-n junction SiNW solar cells that were prepared by assembly of monolayers of silica beads and subsequent DRIE, followed by boron diffusion, and reached an efficiency of 5.3% [715]. In 2012 Oh et al. managed to reduce both Auger and surface recombination in MCEE prepared black Si by using a special chemical treatment to reduce the surface area of the SiNWs by smoothening the nanoscale roughness of the sidewalls and thus reached an excellent efficiency of 18.2% [723]. The authors also suggest that efficiencies above 20% can be reached by optimizing the nanostructure and by improving the passivation of the back while using point contacts. Another promising concept was published by the group of Yi Cui from Stanford University in 2013 and describes the formation of Si nanocones on top of ultrathin Si layers [724]. The RIE fabricated nanocones (Fig. 81) have the advantage of strong light scattering and absorption while the surface area is much smaller in comparison to long wires. Furthermore they used an all-back-contact scheme to reduce Auger recombination losses and reached an overall efficiency of 13.7%.
10.2.2 Substrate variations and random versus organized SiNWs

During the development of nanowire based solar cells, mostly c-Si wafers were used as substrate for growth or etching of wires. Over the last years new processes have been developed to grow SiNWs on cheap substrates like glass [709] or metal foils or to etch SiNWs into multicrystalline deposited Si thin-films on cheap substrates [716]. In order to reach cost competitiveness with industrial scale production, SiNWs need to be realized on substrates that are suitable for existing PV equipment.

The distinction between bottom-up growth and top-down etching are the random distribution and organized distribution of SiNWs respectively. The NW axis direction as well as the diameter can either be controlled or remain random. Depending on the process this control can easily be achieved or needs a very complex treatment. NW orientation and
diameter distribution play an important role for the optical properties of the NW carpet, while the electrical properties are mostly influenced by the diameter.

The diameter of bottom-up VLS grown SiNWs can be narrowed down easily by the size of the initial metal catalyst particles. The orientation of VLS grown NWs on the other hand, can only elaborately be controlled by a very clean environment and the usage of problematic precursors like SiCl$_4$ [701]. On the contrary, mats from randomly oriented SiNWs can also show superior optical properties and they can even be explained by statistical models as Brönstrup et al. have shown [725].

Recently, top-down etched SiNWs are showing a higher relevance for nanostructured solar cells. Both wet-chemical etching as well as reactive ion etching yields highly absorbing randomly shaped SiNWs without using any pre-structuring or lithography steps. The advantage of high absorption is counteracted by the poor electrical quality, since a random etching leads to a large distribution of diameters and severe surface roughness. If the wires are too thin, they can be fully depleted or absorb only a little amount of light, while too thick wires could show a decreased charge carrier separation due to long needed diffusion lengths to the contact. Therefore many groups try to gain control over the SiNW diameter to gain defined electrical properties, without losing the advantage of high optical absorption.

10.3 Current Status, challenges

There are many challenges when it comes to a possible commercialization of SiNW solar cells. One of the main problems of SiNW solar cells is the high surface recombination. Currently, two different approaches try to minimize these effects: The first method is to minimize the surface area by tuning the geometry of the SiNWs, especially the aspect ratio. Here, a combination of electro-optical modeling and experimental investigations is promising. The second approach is the optimization of surface passivation to reduce the recombination. For high aspect ratio structures the atomic layer deposition is the most
valuable technique that is also compatible with PV industrial mass production. For instance, the passivation with ultrathin Al₂O₃ layers is investigated very intensively in the last years and shows promising results.

**10.3.1 Challenges for mass production**

On the way to an integration of SiNWs into commercial mass production many challenges have to be overcome. The large-scale synthesis is still a large problem for both bottom-up and top-down processes. The drawbacks of VLS growth are the needed high-temperature reactors, the typically used catalyst material and the general reactor design, which is limited to substrates with sizes of a few cm² at the moment. Furthermore, an integration into existing PV production lines is a challenge. On the other hand, RIE is a promising technique that can be scaled to large substrates, but here the masking layer of typically used micro- or nanospheres is the problem. A solution to this obstacle could be nanoimprint lithography which could replace the nanosphere mask and offers the possibility of large-scale and fast patterning.

Even if SiNW solar cells reach high-efficiencies while remaining cheaper than typical Si thin-film solar cells, they have to be integrated into a complete PV line including module formation and packaging. Here, a drop-in replacement of typical wafers without the need of new processes and equipment would be the best solution. However, this is mainly ignored in the research community by now. So far, the competition against planar devices, which are extremely advanced because they have been improved with immense investment over the past several decades, remains tough. A large-scale industrial involvement in the development of SiNW solar cells would boost their competitiveness. However, in times of hard competition in the PV market at the moment, the industry mainly concentrates on the further improvement of their running products instead of investing in novel structures. Therefore, academic research needs to show the superior properties of SiNWs in large-scale solar cells.
10.4 Future outlook on promising concepts

Since the field of SiNW solar cell research is still in the early stages of development, there exist several competing PV cell architecture concepts. From the viewpoint of fundamental research, SiNWs are still under intense investigation.

Parallel to the improvement of existing concepts, there is still a large community for innovative and new ideas, such as hybrid inorganic-organic solar cells [726-728], or graphene for Schottky junction solar cells [729] or novel contact materials [730].

SiNW solar cells are still a very complex topic with a multitude of subfields. So far, no concept was able to show its superiority and thus many of them are under investigation concurrently. Here, many challenges remain for both research and industry.

To gain a more detailed overview about the field, we suggest some of the recent reviews by Peng & Lee [731], Kuang et al. [694], Garnett et al. [732], and Ramanujam & Verma [16].

11. GaAs and its related NWs for solar cells

III-V compound semiconductors are very promising materials for NW based PV devices due to their high absorption coefficient (e.g. $10^6$/cm at 0.3 µm for GaAs) and availability of direct bandgaps within the solar spectrum. Aligned NW arrays are very promising building blocks for various nanoelectronic devices, such as nanolasers [733], field-effect transistors [735], light-emitting diodes [736, 737] and field emitters [738,739]. Compared to polycrystalline films, vertically oriented NW arrays are particularly advantageous for PV applications, because the oriented geometry provides direct conduction paths for photogenerated carriers to transport from the junction to the external electrode, thereby resulting in high carrier collection efficiency [740, 741]. Moreover, NW arrays have
significantly smaller optical reflectance and enhanced light absorption in comparison to thin-films due to the foresting effect [742,743]. It is important to note that due to the strain accommodation at the NW sidewalls, NWs are less restricted by lattice mismatch, which provides greater freedom for bandgap engineering and the substrate selection [744]. Thus, a much wider range of material bandgaps may be used in multi-junction NW cells to optimize solar cell efficiency without the restriction of lattice matching in comparison to the planar geometry.

11.1 Basics of GaAs NWs growth

As for GaAs based arrays, in most cases, NWs can be formed via the so-called VLS growth mechanism [695] using different epitaxial techniques, such as MOCVD [745-747], magnetron sputtering [748] or MBE [749-756]. The main stages of the NW growth are following: (i) the formation of a liquid droplet on the substrate surface (for instance, Au or another metal), (ii) the deposition of the desired material onto the surface. The droplet on the surface acts as catalyst, the growth of the NWs is dictated by the diameter and the appropriate place of the droplet. The catalyst in the liquid state should not wet the semiconductor surface, which is necessary for formation of three-dimensional seeding droplets and nucleation of NWs. Additionally, a solution of the catalyst and the semiconductor should have a reasonable melting point (lower than typical growth temperatures). Since NWs feature the predominant direction of growth along the \( [111] \) axis, the wafers with orientation \(<111>\) (for example, Si \(<111>\) or GaAs \(<111>B\)) are used in order to obtain the crystals oriented perpendicularly to the surface. In most cases, at least for MOCVD, magnetron sputtering or MBE, the growth is conducted via so called diffusion driven mechanism, where the NW length exceeds several times the effective thickness of deposited material. In the majority of cases, the dependence of the length (L) of NW on their radius (R) is power law, \( L \sim 1/R \) and \( L \sim 1/R^2 \) [757,758].
Figure 82 shows the typical SEM image and corresponding L(R) dependency for GaAs.

Similar behavior was observed for (Al, Ga)As NWs.

One of the most important features of MBE growth is the ability to precisely control the shape, height, diameter and surface density of the NWs by an appropriate choice of technological parameters by exploring the diffusion induced growth mode, as well as to monitor the formation and time evolution of NWs in situ by the reflection high-energy electron diffraction (RHEED) technique [759]. These peculiarities (i.e. control over growth parameters, doping possibility, growth processes monitoring) allow one to fabricate first PV prototypes based on GaAs NWs [760-762] grown by MBE.

11.2 GaAs NW based PV structures

A coaxial GaAs NWs structure in which a doped NW core is surrounded by a shell of opposite doping type, forming a core-shell p-n junction grown on GaAs<111>B wafer was proposed and successfully realized [760]. Schematic diagram of the MBE grown GaAS nanowire and I-V characteristics are presented in Fig. 83 (a) and (b) respectively.
11.2.1 PV devices based on GaAs NW arrays

It is well known that Si is commonly used n-type doping impurity during conventional MBE. In VLS growth, in contrast, Si incorporation may be amphoteric and both n- and p-type conductivity may appear, depending on Ga or As site substitution [760]. To avoid this, group VI element tellurium was used. In this study, core-shell p-n structures were fabricated by switching from n- to p-type doping during the growth. Tellurium from a GaTe loaded effusion cell was used for n-type doping, and beryllium from an effusion cell was used for p-type doping. PV devices were fabricated in five steps [760]. First, a ∼200 nm layer of SiOx was deposited over the NWs by PECVD. Next, the sample was covered with Shipley S1808 photoresist by spin coating. After the photoresist application, the sample was placed in an oxygen plasma reactive ion etch chamber to remove the photoresist from the tip of the oxide-covered nanowires. Next, using the photoresist as an etch mask, the oxide was removed from the tip of the NWs using buffered HF etch followed by acetone rinse to remove the photoresist. This process isolates the contact to the tips of the NWs and prevents direct contact to the thin-film that grows simultaneously between the NWs. Either opaque contacts or transparent contacts were deposited on top of the NWs for top contact. The procedure was finalized by the contact deposition on the back of the wafer. As a result, several PV prototypes were synthesized with a maximum conversion efficiency of 0.83%. Corresponding I-V data taken in the dark and under illumination is presented in Fig.83 (b).
Fig. 83 (a) Schematic diagram of the MBE grown p-n core-shell type GaAs nanowire grown by switching doping type during the growth, (b) I-V curves of optimized sample in dark and illuminated conditions. The GaAs nanowire samples are grown by MBE on GaAs<111>B wafer. Si is used as n-type dopant. In VLS growth, Si incorporation may be n-type or p-type depending upon Ga or As site substitution. Therefore, group VI element tellurium (Te) from a GaTe loaded effusion cell is used for n-type doping, and beryllium from an effusion cell is used for p-type doping. A maximum efficiency of 0.83% has been obtained. Figure 83 from [760], Josef A. Czaban, David A. Thompson and Ray R. LaPierre, GaAs Core–Shell Nanowires for Photovoltaic Applications, Nano Lett., 9 (2009) 148. Copyright © 2008 American Chemical Society. Permission granted.

Another PV prototype concept was proposed in Ref. [756]. Here, GaAs p-type NW arrays are grown on the n-type GaAs<111>B wafer at different wafer temperatures. Additionally, to prepare the p-n junction, the spaces between the NWs are filled with insulating photoresist (Poly (methyl methacrylate) or PMMA) via spin coating. In this particular case, PMMA was used for electrical insulation and contact mechanical support. After photoresist deposition, the sample surface is treated in oxygen plasma until the tips of GaAs NWs are exposed. Conventional ohmic contacts for the backside of n-type wafer are fabricated by electron-beam evaporating of AuGe (30nm) and Ni/Au (10/150nm) combination having resulting contact resistance \(\sim1\times10^{-6}\)Ohm/cm\(^2\). After each stage, the samples are studied by applying the SEM technique as shown in Fig.84 (a-c), together with schematics of the device structure. I-V characteristics are measured using a Keithley 238
source meter (Fig.84d). The samples are placed on a Cu base from backside of the wafer; a metallic sharp tip (D~0.5mm) is used as top contact to the NWs/PMMA array. The efficiency is determined by illuminating the structures with one sun illumination. For the given geometry, the highest conversion efficiency 1.65%, with $J_{sc}$ of 27.4mA/cm$^2$ and the $V_{oc}$ of 245 mV and fill factor of 25% is achieved when the substrate growth temperature was set at 550°C.

![Fig.84. SEM images taken at different stages of device structure preparation, (a) as-grown GaAs NWs array, (b) after insulating photoresist (PMMA) deposition for electrical isolation and mechanical support, (c) top view of the resulting structure (after oxygen plasma treatment), and (d) schematic view of the device testing structure.](image)

The MBE growth of beryllium-doped GaAs NWs on n-type GaAs<111>B wafer is carried out at wafer temperature 550°C with GaAs growth rate at 1 monolayer/s. An efficiency of 1.65% has been obtained due to a low fill factor of 0.25. From [761], G.E. Cirlin, A.D. Bouravlev, I.P. Soshnikov, Yu.B. Samsonenko, V.G. Dubrovskii, E.M. Arakcheeva, E.M. Tanklevskaya, and P. Werner, Photovoltaic Properties of p-type GaAs Nanowire Arrays Grown on n-Type GaAs(111)B wafer, Nanoscale Res Lett., 5(2010)360. Permission granted.

Different approach was utilized in Ref. [762,763] to combine GaAs and polymer films. These hybrid solar cells were fabricated by spin-coating poly (3-hexylthiophene) (P3HT) polymer onto vertically aligned n-type GaAs NW arrays synthesized by MBE [762] and MOCVD [763]. In both approaches, GaAs<111>B wafer was used. In the last case,
patterned GaAs nanopillars were used as a PV prototype base. According to the scheme [762], the highest occupied molecular orbital (HOMO$_{P3HT}$) and lowest unoccupied molecular orbital, (LUMO$_{P3HT}$) for P$_3$HT is $-4.76$ eV and $-2.74$ eV, respectively. The electron affinity of GaAs is $\chi_{GaAs} \approx 4.07$ eV. Therefore, GaAs NWs are suitable as electron acceptor, and P$_3$HT as the electron donor. For this concept, 1.04% and 1.44% conversation efficiencies were achieved, respectively, showing alternative and less expensive approach to fabricate NWs based solar cells.

Another way to increase the solar cells efficiency was demonstrated in [764] where p–n junction GaAs NW solar cell devices of two types consisting of ITO contact dots or opaque Au finger electrodes, were investigated. Lateral carrier transport from the NWs to the contact fingers was achieved via a p-type GaAs surface conduction layer. NWs between the opaque contact fingers had sidewall surfaces exposed for passivation by sulphur. Using this approach, the relative cell efficiency was increased by 19% upon passivation. Before and after passivation, efficiency was 1.8% and 2.04% respectively.

It is known that Au-assisted VLS growth can lead to an unintentional Au contamination [765]. To overcome this disadvantage, it is desirable to utilize the same material serving the NWs growth catalyst. One of the major steps towards the new PV prototypes was an introduction of self catalyzed NWs growth where the metal droplet (catalyst) is a seed particle that is a constituent of the NW itself, e.g. Ga for GaAs NWs growth [766-771]. A key point is the formation of liquid Ga nanoparticles at the initial stage in the openings of SiO$_x$ grown on the GaAs$^{<111>B}$ wafer [766], or in a native oxide layer on the Si$^{<111>}$ wafer [767].

In case of GaAs/Si self catalyzed NWs, the growth procedure is as follows: before introduction into the growth chamber, the wafers are chemically treated in HF (10% in DI water) for 1 min, and then rinsed in de-ionized water. Before the growth of NWs, the wafer
temperature is increased to the desired value within the range 560ºC-630ºC, and is kept constant during the whole growth process. In this temperature window, a native oxide layer on Si<111> wafer loses continuity, and openings (i.e. the holes penetrating through the oxide towards the wafer surface) are formed. The surface density of those openings depends on the temperature. Above 630ºC, the oxide layer is completely desorbed, as detected by the corresponding transformation of RHEED pattern. After the formation of openings, the Ga flux is supplied to the surface for several seconds, while the arsenic shutter is closed. This initiates the formation of Ga droplets in the openings. When the arsenic flux is switched on, the NW growth is started after an incubation time. The latter is clearly detected by the transformation of the RHEED pattern and typically amounts to 2-10s, depending on the temperature. During the NW growth, the RHEED pattern features pronounced 3D spots of cubic zinc blende phase regardless of the temperature. The spot structure does not change during the whole growth process excluding the very final stage after the Ga shutter is closed.

The ability to position regularly the group III droplets in the holes patterned in the oxide film (by using, e.g. e-beam lithography or focused ion beam techniques) is very attractive to tune the spacing between the NWs, and hence to maximize light absorption. Additionally, the self-assisted process is compatible with III–V integration on Si platform, which will lead to lower cost PV devices. Possible device structures based on self-catalyzed GaAs NWs are presented in the next section.

11.2.2 PV devices based on single GaAs NW

One of the first demonstrations of the self-catalyzed p-i-n radial GaAs NWs applied to the PV devices was presented in [771], where the fabrication procedure was as follows: GaAs <111>B wafers coated with a sputtered 10nm thick SiO₂ were used as substrates. The NWs growth was carried out at a nominal GaAs growth rate of 0.25Å/s, arsenic partial pressure of 2x10⁻⁶ mbar (Ga rich conditions), a temperature of 630ºC. The core of the p-i-n NW junction
was p-type. This was achieved by adding a Si flux during the NWs growth. As it was mentioned above, Si is an amphoteric impurity in GaAs, and its incorporation can lead to n- or p-type doping, depending on whether it is incorporated in As or Ga sites, i.e. incorporation of Si in As (Ga) site results in p-GaAs NW (n-GaAs NW). In the case of Ga-assisted GaAs NWs growth, incorporation of Si mostly results in a p-type doping [771]. To overcome this problem, the growth was stopped and the conditions were changed toward planar MBE growth. Arsenic partial pressure was increased, which resulted in the crystallization of the Ga droplet. The fabrication of the p-i-n junction continued by the growth of an intrinsic (i) and an n-type layer on the facets of the nanowires. For this purpose, the temperature was lowered to 465°C. These conditions had previously been shown to be ideal for growth on {110} nanofacets [772]. For this growth conditions, due to the lower temperature and higher As$_4$ beam flux, the incorporation of Si leads to n-type layer [773]. After the growth, the p-i-n GaAs NW structures were transferred on an oxidized c-Si wafer. The p-type core of the NW was contacted by first etching a section of the n-type and intrinsic layers of the NW. The etching was performed with a citric acid solution. Next, a Pd/Ti/Au (70/10/120 nm) layer was evaporated to form an Ohmic contact with the p-type core. A second lithographic step was realized with the purpose of contacting the n-type shell. For this, a Ti/Au (10/240 nm) layer was used. A sketch of the contacted p-i-n nanowire structure is presented in Fig. 85(a). There the three coaxial layers can be observed, as well as the contacting between the inner and exterior layers. SEM of a real structure is shown in Fig. 85(b).
To further characterize the p-i-n junction, the light emitted by the NW in forward bias was measured (which corresponds to the regime in which the junction works as a light emitting diode) at room temperature. The emission peak at 1.42 eV is in good agreement with the bandgap of GaAs. The existence of electroluminescence at room temperature constitutes a further proof of the quality of the p-i-n junction in the NW, crystallinity and optical quality.

The efficiency of the NW device was measured under 1.5 AM illumination conditions. The total efficiency was calculated by dividing the maximum generated power density by the total incident energy density at 1.5 AM. The total area considered was the projected area of the p-i-n junction. For the best sample, a value of 4.5% was obtained with fill factor equal to 0.65.

Very impressive result was obtained recently based on the GaAs single NW solar cells, grown on a c-Si wafer, where the p-type is contacted through a highly doped wafer and the n-type through a transparent top contact [774]. Here, the NWs were grown on oxidized Si<111> with 100nm apertures using a self-catalyzed method. The p-doping of the core was achieved by adding a flux of beryllium during axial growth. The shell was obtained at lower
wafer temperature, the procedure used before in Ref. [771], and the n-type doping was obtained by adding Si at this growth stage. Next, SU-8 was spun onto the wafer. An oxygen plasma etching was then performed to expose the NW tip. The top contact was defined by electron-beam lithography followed by evaporation of ITO, and the bottom contact was obtained by gluing Ag to the back side of the structure. In Fig. 86 (a-d) a sketch of the device structure, corresponding microscope images, and I-V characteristics are presented.

Fig. 86. (a) Schematic diagram of the vertical p-i-n type single nanowire device connected to a p-type c-Si wafer by epitaxial growth, (b) Left side: doping structure of the GaAs nanowire. The p-type core is in contact with the doped c-Si wafer and the n-type shell is in contact with the ITO. Right side: SEM image of a GaAs nanowire
solar cell before adding the top contact, (c) SEM images of the device seen from the top electrode, (d) I-V characteristics of the device in the dark and light under AM 1.5G illumination. From [774], Peter Krogstrup, Henrik Ingerslev Jørgensen, Martin Heiss, Olivier Demichel, Jeppe V. Holm, Martin Aagesen, Jesper Nygard, Anna Fontcuberta i Morral, Nature Photonics 7(2013)306. Nature publishing group, copyright © 2013 Macmillan Publishers Limited, Permission granted.

The authors observed a remarkable boost in absorption in single NW solar cells and explained this observation as due to a vertical configuration of the NW, and by a resonant increase in the absorption cross-section. For the best case, the PV device exhibits a J_{sc} of 180mA/cm² when normalized to the projected area. This leads to an apparent efficiency of 40%, which is beyond the S-Q limit [22], and opens a new route to third generation solar cells.

11.3 PV devices based on other III-V material NW arrays

As concern to another III-V materials used for the NW based solar cells prototypes, one should mention InP/Si<111> NWs double-junction structure grown by MOVPE [775], InGaAs/Si<111> NWs using MOVPE [776], MOCVD grown InGaP/GaAs<111>B NWs [777], GaAsP/Si<100> MOCVD grown NWs [778], GaAsP/Si<111> NWs using MBE [779] etc. More detailed information can be found here [780]. But one of the results has to be outlined separately. The record efficiency for a Au-assisted InP axial p–i–n nanowire array on an InP<111>B substrate, which was achieved recently an efficiency of 13.8% [781]. This high value is attributed to the use of the patterned array, more optimal geometry, and lower SRV in indium phosphide material.

An important aspect, aiming to increase the absorption of the light in the NW based PV structure, is the use of a combination of several materials inside a NW. Among the different geometries (e.g. core/shell homo- and heterostructures, or double-junction structures), a structure consisting of the nanostructures with combined dimensionality, namely QD inside a nanowire, has additional advantages, such as spreading of the absorption spectrum and, due to the small sizes, facilitating of the strain relaxation. Recently, a
remarkable progress was achieved in this field. In Fig. 87 (a) and (b), typical transmission electron microscopy for the InAsP/InP/InAsP [782] and AlGaAs/GaAs/AlGaAs [783] QD inside a NW combined structures are presented. These nano insertions have typically ~5-20 nm size and exhibit zero-dimensional behavior. Moreover, these structures are optically bright up to the room temperature, demonstrating outstanding potential for PV applications.

![Transmission electron microscope images for the quantum dot inside a nanowire structure](image)

(a) InAsP/InP/InAsP [from 782], and (b) AlGaAs/GaAs/AlGaAs [from 783]. The details of the grown structures are presented in the corresponding references. Figure 87 (a) from [782], Maria Tchernycheva, George E. Cirlin, Gilles Patriarche, Laurent Travers, Valery Zwiller, Umberto Perinetti, and Jean-Christophe Harmand, Growth and Characterization of InP Nanowires with InAsP Insertions, Nano Lett., 7(2007)1500. Copyright © 2007 American Chemical Society. Permission granted. Figure 87 (b) from [783], V. N. Kats, V. P. Kocharshik, V. V. Platonov, T. V. Chizhova, G. E. Cirlin, A.D. Bouravlev, Yu B Samsonenko, I. P. Soshnikov, E. V. Ubyivov, J. Bleuse, H. Mariette, Optical Study of GaAs quantum dots embedded into AlGaAs nanowires, Semicond. Sci. Technol., 7 (2012) 015009. Copyright ©2012 IOP Publishing Ltd. Permission granted.

### 11.4 Future outlook

There is a strong interest in the fabrication of novel PV devices based on III-V material NWs, in particular, GaAs NWs. These structures may provide a lower cost, higher efficiency devices in PV market. Additionally, different materials combination within a single, defect-free NW, may lead to higher absorption efficiency. Nevertheless, further investigations are required to make NWs based PV large-scale solar cell commercial devices. For better understanding of the processes involved in PV conversion, intensive numerical simulation and theoretical approaches with an emphasis on optimizing the NW design has
been performed [784, 785]. Important factors, such as surface charge density, SRV, doping concentration, and NW geometry were investigated in detail.

The particular interests in this area are: (i) the variation in $V_{oc}$ with NW diameter and change in $J_{sc}$ with tip length indicates the importance of a monodisperse distribution in NW dimensions, (ii) the minimum NW diameter should be greater than the bulk and surface depletion widths, which are determined by the doping concentrations [784] and (iii) importance of a core-shell geometry of NW solar cells [785]. Based on the analysis of numerous experimental and theoretical data in this area, the following attributes should be considered for the use of these NWs for PV applications [780]:

(i) Controlled NW morphology
(ii) Stacking-fault-free crystalline structure
(iii) Orthogonal NWs with optimum diameter, and length to maximize optical absorption
(iv) Patterned arrays using cost-effective processes (perhaps nanoimprint lithography)
(v) Dimensions below the critical thickness or critical diameter to avoid misfit dislocations, which is very important, in particular, when III-V material NWs are grown on c-Si wafers [786]
(vi) Removal of catalyst droplets to avoid reflection loss and/or Schottky barrier contacts at the tip of NWs, and possible elimination of Au as a catalyst due to deep level defects
(vii) Controlled doping for p–i–n junctions
(viii) Surface passivation

12. Conclusions

We have reviewed the development and current state of inorganic materials based PV, with a focus on planar devices and recent developments involving a range of nano-materials. c-Si based traditional solar cells have dominated the solar cell market for decades, and are expected to continue playing a dominant role, in particular with recent developments towards low-cost fabrication. At the same time, other technologies have emerged to address the limitations and progress the state-of-the-art. For example, a method to overcome optical
shadowing losses completely is to use a back junction design. These cells have shown efficiencies as high as 24.2%. An important concept is a c-Si based BHJ solar cell. Very high-efficiency of 25.6% has been reported [246] for BHJ solar cells, and recent simulation study shows an efficiency of >26%.

Another area of intensive focus is the integration of III-V or metal halide perovskite based materials on c-Si. This may provide a cost breakthrough for PV technology, unifying the low-cost of c-Si and the efficiency potential of III-V/c-Si or perovskite/Si multi-junction solar cells. However, despite the promising potential of these structures, the integration of III-V on c-Si has been challenging due to mismatches in lattice constants and thermal parameters of III-V compounds and c-Si, whereas for perovskite/Si cells, the stability of the perovskite top cell currently appears to be the greatest challenge.

An important challenge for the larger PV community has been to cross the S-Q limit of solar cell efficiency (29% in case of c-Si). One possible way to achieve this, besides the use of multi-junction devices based on well-established single-junction cells as mentioned above, is to use quantum dots. This may include the use of a quantum dot Si absorber layer, where charge-carriers are collected before they are able to thermalize (hot carrier effect).

Another potential method is to develop solar cells using nano-crystalline Si solar cells. The use of up-conversion and plasmonics has also garnered immense interest. However, much further research work needs to be done here to approach the theoretically predicted potential.

Among non-Si based inorganic solar cells, one technology that has been adopted by the industry has been CIGS solar cells. At the same time, CZTSSe PV technology has experienced rapid growth both in conversion efficiency and materials understanding, and future breakthroughs in fabrication methodologies are expected to make this technology a serious commercial contender. At the same time, the work carried out over the last few years
in perovskite and CdTe solar cells has been significant for both planar and nanostructured solar cells.

In terms of very nascent technologies, the field of SiNW solar cell research is still in the early stages of development, and there exist several competing PV cell architecture concepts. SiNWs are still under intense investigation, and many challenges remain for both research and industry. Similarly there is a strong interest in the fabrication of novel PV devices based on III-V material NWs, in particular, GaAs NWs. These structures may provide lower cost, higher efficiency devices for the PV market. Additionally, different materials combinations within a single, defect-free NW, may lead to higher absorption efficiency. Nevertheless, further investigations are required to make NWs based PV large-scale solar cell commercial devices.

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REFERENCES


[37] Fig. 2.3 Courtesy to McMaster University, Hamilton, ON, Canada.


[89] https://www.itri.org.tw/eng/Content/MsgPic01/Contents.aspx?SiteID=1&MmmID=620170236611417772&MSid=620170245320003156


P.J. Verlinden, R.A. Sinton, K. Wickham, R.A. Crane, and R.M. Swanson, “Backside-contact silicon solar cells with improved efficiency for the ’96 world solar challenge”,


dominority carrier lifetimes in n-type multicrystalline silicon”, Applied Physics Letters,


[213] M. Hermle, F. Granek, O. Schultz, and S. W. Glunz, „Analyzing the effects of front-
surface fields on back-junction silicon solar cells using the charge-collection
probability and the reciprocity theorem”, Journal of Applied Physics 103, 054507
(2008)

[214] C. Reichel, F. Granek, J. Benick, O. Schultz-Wittmann, S. W. Glunz, „Comparison of
Emitter Saturation Current Densities Determined by Injection-Dependent Lifetime
Spectroscopy in High and Low Injection Regimes”, Progress in Photovoltaics:


[216] F. Granek, M. Hermle, C. Reichel, A. Grohe, O. Schultz-Wittmann, S. Glunz,
“Positive effects of front surface fielding high-efficiency back-contact back-junction
n-type silicon solar cells”, 33rd IEEE Photovoltaic Specialist Conference, San Diego,
CA (2008).

[217] F.Granek, M. Hermle, D. M. Huljić, O. Schultz-Wittmann and S. W. Glunz,
“Enhanced lateral current transport via the front n'-diffused layer of n-type high-
efficiency back-junction back-contact silicon solar cell”, Progress in Photovoltaics 17,
47-56 (2009).

optimization study of industrial n-type high-efficiency back-contact back-junction


[221] C. Reichel, M. Bivour, F. Granek, M. Hermle, S. W. Glunz, „Improved diffusion
profiles in back-contacted back-junction Si solar cells with an overcompensated
boron-doped emitter”, physica status solidi (a), Vol. 208, No. 12, 2871–2883, (2011)


C. Reichel, F. Granek, M. Hermle, S.W. Glunz, „Back-contacted back-junction n-type silicon solar cells featuring an insulating thin film for decoupling charge carrier collection


Mews, Mathias, Tim F. Schulze, Nicola Mingirulli, and Lars Korte. "Hydrogen plasma treatments for passivation of amorphous-crystalline silicon-


Haschke, J. and Jogschies, L. and Amkreutz, D. and Korte, L. and Rech, B. "Polycrystalline silicon heterojunction thin-film solar cells on glass exhibiting


Lu M, Das U, Bowden S, Birkmire R. Rear surface passivation of interdigitated back contact silicon heterojunction solar cell and 2D simulation study. Proc of 33rd IEEE PVSC San Diego (USA) 2008;11-5.


Silicon Heterojunction for Advanced Rear Contact Cells: Main Results of the  

O'Sullivan BJ, Bearda T, Qiu Y, Robbelein J, Gong C, Posthuma NE, Gordon I,  
Poortmans J. Interdigitated rear contact solar cells with amorphous silicon  

Amorphous Crystalline silicon Heterojunction (BACH) photovoltaic device. Proc  
of 34th IEEE PVSC Philadelphia (USA) 2009;1767-70.

Chowdhury ZR and Kherani NP. Back amorphous-crystalline silicon  
heterojunction (BACH) photovoltaic device with facile-grown, oxide - PECVD  


http://www.pv-tech.org/news/back_contact_hit_solar_cell_from_  
panasonic_pushes_efficiency_record_to_25.6

Mac Donald D, Rougieux F, Cuevas A, Lim B, Schmidt J, Di Sabatino M,  
Geerligs, LJ. Light-induced boron-oxygen defect generation in compensated p-  

Tucci M, Serenelli L, De Iuliis S, Izzi M, de Cesare G, Caputo D. Contact  
Formation on a-Si:H/c-Si Heterostructure Solar Cells. Physics and Technology of  
Armophous-Crystalline: Springer Ed 2011;321-75.

Tucci M, Serenelli L, De Iuliis S, Izzi M, de Cesare G, Caputo D. Back contact  
formation for p-type based a-Si:H/c-Si heterojunction solar cells. Physica Status  

Tucci M, della Noce M, Bobeico E, Roca F, de Cesare G, Palma F. Comparison  
of amorphous / crystalline heterojunction solar cells based on n and p type  

Diouf D, Kleider JP, Desrues T, Ribeyron PJ. Interdigitated Back Contact a-  
Si:H/c-Si Heterojunction Solar Cells Modelling: Limiting Parameters Influence  
on Device Efficiency. Proc of 23rd EUPVSEC Valencia (Spain) 2008;1949-52.

Caputo D, de Cesare G, Palma F, Tucci M, Minarini C, Terzini E. Investigation  
of amorphous silicon compensated materials over a wide range of dopant  

Thickness-dependent conductivity and photoconductivity of hydrogenated  

Tucci M. Optimization of n-doping in n-type a-Si:H / p-type textured c-Si heterojunction for photovoltaic applications. Sol En Mat Sol Cells 1999;57:249-57.


http://www.esrf.eu/computing/scientific/xop2.1/


Meier, M., Paetzold, U.W., Ghosh, M., Zhang, W., Merdzhanova, T., Jost, G., Sommer, N., Michard, S., Gordijn, A., Fabrication of light-scattering multiscale
textures by nanoimprinting for the application to thin-film silicon solar cells,
IEEE Journal of Photovoltaics, 2014; 4 :772-777

Management Using Periodic Textures for Enhancing Photocurrent and
Conversion Efficiency in Thin-Film Silicon Solar Cells. Mat Res Soc Symp Proc
2013; 1536:3-15

Ganapati E, Miller OD, Yablonovitch E, Light trapping textures designed by
electromagnetic optimization for subwavelength thick solar cells, IEEE Journal
of Photovoltaics 2014; 4:175-182.

Atwater HA, Polman A. Plasmonics for improved photovoltaic devices. Nature
Materials 2010; 9:205-213

Battaglia C, Escarre J, Soderstrom K, Charriere M, Despeisse M, Haug FJ, Ballif
C. Nanomoulding of transparent zinc oxide electrodes for efficient light trapping

Stencil-nanopatterned back reflectors for thin-film amorphous silicon n-i-p solar
cells. Proc 38th IEEE PVSC Austin 2012; 694-696

de Jong MM, Sonneveld PJ, Baggerman J, van Rijn CJM, Rath JK, Schropp REI.
Utilization of geometric light trapping in thin film silicon solar cells: simulations


efficiency-record_100016505/#axzz3EJGmgHsk (accessed Mar 2016)

Li HBT, Franken RH,Rath JK, Schropp REI. Structural defects caused by a rough
substrate and their influence on the performance of hydrogenated nano-crystalline
349

Andrew Barnabas Wong, Sarah Brittman, Yi Yu, Neil P. Dasgupta, and Peidong
Yang, Core–Shell CdS–Cu2S Nanorod Array Solar Cells, Nano Lett., 2015, 15
(6), pp 4096–4101.

Kuang Y, van der Werf CHM, Houweling ZS, Schropp REI. Nanorod solar cell
(1-3).

GeiBendörfer S, Vehse M, Voss T, Richters JP, Hanke H, von Maydell K, Agert
C. Integration of n-doped ZnOnanorod structures as novel light-trapping concept


Gunawan O et al., Electronic properties of the Cu2ZnSn(Se,S)4 absorber layer in solar cells as revealed by admittance spectroscopy and related methods, Appl. Phys. Lett. 2012;100:253905.


Han YX, Yang CL, Sun YT, Wang MS, Ma XG. The novel optical properties of CdS caused by concentration of impurity Co. Journal of Alloys and Compounds 2014;585:503-9


Lee YJ, Ruby DS, Peters DW, McKenzie BB, Hsu JWP. ZnO nanostructures as efficient antireflection layers in solar Cells, Nano Lett 2008;8:1501-5.


