IMPROVEMENT OF POLYMORPHOUS/CRYSTALLINE HETEROJUNCTION SOLAR CELLS USING LOW TEMPERATURE SCREEN-PRINTED PASTES

Y. Veschetti[1], J.-C..Muller[1], J. Damon-Lacoste[2], P. Roca i Cabarrocas[2], A. S. Gudovskikh[3], J.-P. Kleider[3], P.-J. Ribeyron[4], E. Rolland[4]
[1]PHASE-CNRS (UPR 292), 23 rue du Loess, BP20, F-67037 Strasbourg Cedex 02, France.
[2]LPICM (UMR 7647, CNRS) Ecole Polytechnique, F-91128 Palaiseau Cedex, France, [3] LGEP (UMR 8507, CNRS), Universités Paris VI et XI, Ecole Supérieure d'Électricité, 11 rue Joliot-Curie, Plateau de Moulon, F-91192 Gif-sur-Yvette Cedex, France, [4]CEA-Grenoble, 17 rue des Martyrs, F-38054 Grenoble cedex 9, France

ABSTRACT

An alternative way to conventional solar cell process is to develop a low temperature process using hydrogenated amorphous silicon (a-Si:H) thin film deposited by PECVD on bulk crystalline silicon. The French national project "SiNERGIES" aims to improve polymorphous/crystalline heterojunction (a-Si:H/pm-Si:H/c-Si) on p-type crystalline silicon (c-Si) to achieve large area solar cells for industrial application. We present the advancement of the project, focusing on low temperature screen-printed pastes (LT-SP) as well as the analysis of the pm-Si:H/c-Si interface quality. Up to now, solar cells of 25 cm² area using CZ (Si) substrate achieved efficiency close to 13.5% with a maximum fill factor of 70% with LT-SP from Dupont MCM. A simulation study gives insight into the possible improvements.

INTRODUCTION

The rapid growth of photovoltaic industry leads to develop new structures, mainly on p-type c-Si wafer. The amorphous/crystalline heterojunction solar cells (a-Si:H/c-Si) produced in Japan by Sanyo on c-Si (FZ) have already shown record efficiencies on n-type silicon [1]. These structures also called Heterojunction with Intrinsic Thin-layer (HIT) possess many advantages: high open-circuit voltage values, low saturation current, and low processing temperatures [2]. Furthermore, a-Si:H/c-Si structures are well adapted for the reduction of wafer thickness due to the low mechanical stresses induced by the low temperature process.

The aim of the "SiNERGIES" project is to evaluate the potential of a-Si:H/c-Si solar cells on p-type substrate for a possible application on thin c-Si or mc-Si wafers (W<200μm). The experimental study presented in this paper will be focused on the development of a front side heterostructure on p-type silicon (CZ) 25 cm² using low-temperature screen printed paste on TCO. Results are analysed through different characterisation techniques (spectral response SR, capacitance-voltage (C-V), and capacitance-temperature (C-T) measurements). A simulation study using the software AFORS-HET [3] gives a better understanding and allows to propose different ways of improvements.

EXPERIMENTAL

Our heterojunction solar cells were fabricated on p-type c-Si substrates (<100> oriented, W=300μm, ρ=14-22 Ω.cm). After a conventional chemical cleaning process, a full aluminium screen-printed layer was deposited and annealed in an IR belt furnace for back contact formation. A particular attention was paid to the front heterojunction interface where we used a thin undoped hydrogenated polymorphous silicon (pm-Si:H) layer instead of the more conventional a-Si:H one. Indeed, it has been shown in previous papers that pm-Si:H has a lower defect density than a-Si:H, and that it provides outstanding passivation properties [4, 5]. A subsequent phosphorus doped a-Si:H(n) emitter layer was deposited onto the pm-Si:H. Both pm-Si:H and a-Si:H layers were deposited by means of a capacitively-coupled PECVD system at an RF frequency of 13.56 MHz under various conditions [6]. The thickness of the pm-Si:H and a-Si:H(n) layers, as deduced from spectroscopic ellipsometry measurements is 3 nm and 12 nm, respectively. A 95 nm thick TCO anti-reflection layer was deposited by DC- magnetron sputtering. Finally, a low-temperature silver paste (Dupont MCM) was screen-printed onto the TCO layer, and annealed at 200°C for front contact formation. Apart from the back contact treatment, the whole process was performed at very low temperature (T<250°C). The experimental study is focused on two main parameters: the interface quality and the contacts quality. In order to compare the potential of this low-temperature process, some additional cells were made according to the industrial standard process, using the same CZ c-Si wafer with the same Al screen-printed back contact. For these standard cells, the emitter was obtained from POCl3 diffusion (40Ω/), and the front surface was processed using deposition of a SiN layer and screen-printed Ag contacts.

RESULTS AND DISCUSSION

A batch of wafers was performed under the conditions described above. All the processed cells were analysed by I-V measurements.
To confirm the correct calibration of our simulator, the best cell was measured at Fraunhofer institute (FhG.Callab).

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	Voc(mV)	Jsc(mA/cm²)	FF(%)	η(%)
Average	611.0	31.8	65.8	12.80
P21 (calLab)	613.4	31.2	70.0	13.50
Ref cell P10 (calLab)	617.9	32.4	76.5	15.31

Table I: I-V results of the first batch for the a-Si:H/pm-Si:H/c-Si and reference solar cells.

Table I shows the difference between the efficiency of the reference cell P10 and that of the a-Si:H/pm-Si:H/c-Si cell P21. The average fill factor value remains too low to achieve a satisfactory efficiency. From the I-V curve (fig.1), we observed a high series resistance value which probably comes from the screen-printing step.

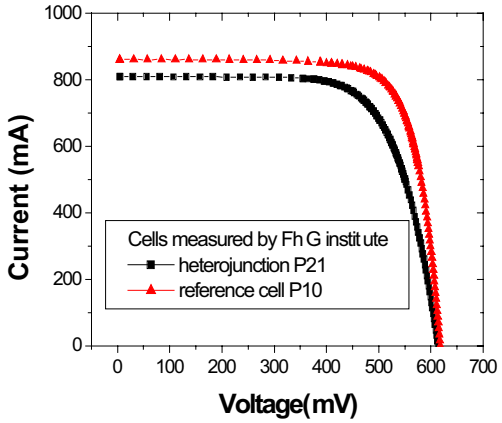

Fig.1: I-V characteristics of the a-Si:H/pm-Si:H/c-Si and reference solar cells.

In order to test our screen printed metallization, we used the Transition Line Model method (TLM). This well-known technique allows to extract the contact resistivity between the TCO layer and the metallization itself. The value of the contact resistance for the front silver paste deposited on TCO after annealing was $Rs=2\times10^{-2}$ Ω.cm². This value is rather high and should be ideally lowered. Nevertheless, it remains comparable to classical screen printed pastes on conventional solar cell process. The paste resistivity is a more important issue. Indeed, the measured resistivity was 4×10^{-5} Ω.cm which is one order magnitude higher than for conventional high temperature pastes. A modelisation of the series resistance clearly indicates that the fingers are responsible for the low fill factor (65% average). Possible improvements of the paste resistivity are tested in our laboratories.

The loss in the short-circuit current (Jsc) is investigated through the spectral response and front side reflectivity measurements. Fig.2 shows the Internal Quantum Efficiency (IQE) spectrum for both cells (a-Si:H/pm-Si:H/c-Si P21 and reference P10) deduced from the external quantum efficiency (EQE) and the reflectivity R from:

$$IQE = \frac{EQE}{1-R} \quad . \quad (1)$$

It appears that the deposited thin film emitter induces more recombination than a highly doped standard emitter in the wavelength range between 300 nm and 600 nm. The thickness of the amorphous layer (12 nm) is probably too high and needs to be reduced. We observed a similar efficiency for wavelengths between 600 nm and 800 nm. Nevertheless a difference of IQE occurs between 800 nm and 1050 nm which cannot be explained by a higher recombination rate in the heterojunction solar cell because the same type of wafer was used for both types of solar cells.

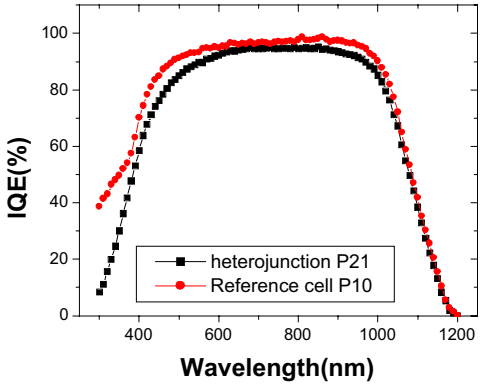

Fig.2: Internal quantum efficiency for the a-Si:H/pm-Si:H/c-Si and reference cells.

A possible explanation is related to the absorption of the TCO anti-reflective layer which is not considered in Eq.(1). Ellipsometry measurements (n,k) of the TCO layer on glass substrate were performed after deposition. Figure 3 shows the optical losses of the TCO layer (absorption and reflectivity).

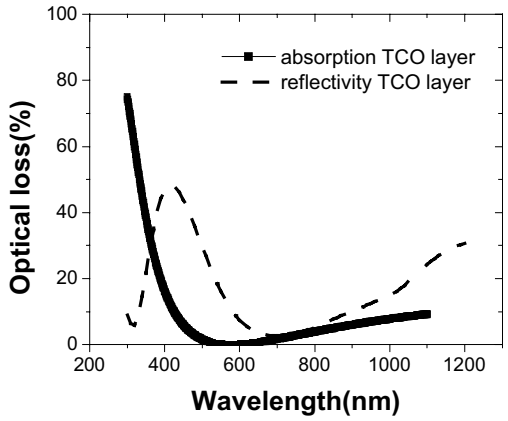

Fig.3: Optical losses in the TCO layer (absorption and reflection).

The increase in the TCO absorption between 700 nm and 1100 nm clearly explains the difference in the IQE. The IQE in the long wavelength range (λ>1000 nm) is limited by the back surface recombination for both structures. The TCO absorption also strongly limits the efficiency at short wavelengths (λ<400 nm).

The analysis of interface quality was performed using capacitance versus temperature measurements. Usually, in the C-T curve, two steps can be observed, that are shifted to higher temperatures when increasing the measurement frequency. The first one occurs at low temperature (100 K - 200 K) and is related to the activation of the transport in the amorphous layer. The second step is caused by trapping-detrapping of charge carriers at interface states and occurs for T>200 K [7,8].

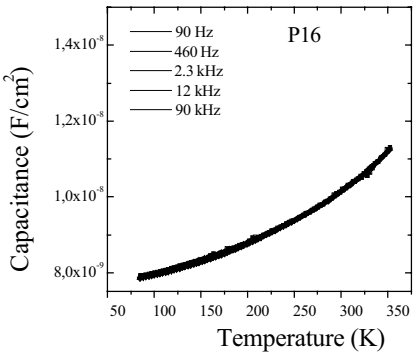

Fig.4: Temperature dependence of the capacitance of a good quality a-Si:H/pm-Si:H/c-Si heterojunction solar cell.

The measurements of the a-Si:H/pm-Si:H/c-Si samples (Fig.4) reveal a smooth increase of the capacitance independently of the frequency, that is related to the temperature dependence of the Fermi level position in the materials, but no step in the capacitance is detected at T>200 K. From numerical modelling, it has been shown that the absence of the high temperature capacitance step means that the interface state density D_{it} is lower than 10^{12}cm² [8]. As a consequence, we can conclude that the passivation of the interface using the thin pm-Si:H undoped layer is satisfactory. Further characterisation is necessary to determine the exact value of D_{it}.

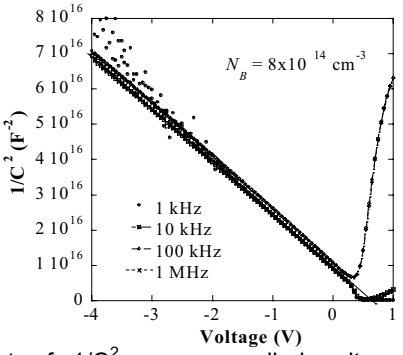

Fig.5: Plot of $1/C^2$ versus applied voltage at room temperature for different frequencies

Additional C-V measurements were performed to evaluate the interface quality and to measure the doping density in the c-Si substrate. Figure 5 shows that the plot of $1/C^2$ versus bias voltage is linear and independent of the frequency in the reverse bias range, and the intercept with the bias axis gives a value (≈ 0.7 V) which is reasonable owing to the position of the Fermi level in both materials and to the conduction band offset [7].
These features also support the good interface quality of our structures. The doping density (N_B) in the bulk c-Si was deduced from:

$$\frac{C}{S} = \sqrt{\frac{q\varepsilon N_B}{2(V_{bi}-V)}} \qquad (2)$$

where ε is the dielectric permittivity, V_{bi} is the built-in potential, V is the applied bias, S is the cell area and q the absolute value of the electron charge. We found N_B=8x10^{14}cm^{-3}, which is consistent with the resistivity of the wafer (14-22 .cm).

POSSIBLE IMPROVEMENTS

We decided to investigate the limiting factors of the heterojunction solar cells by means of a simulation study, using the AFORS-HET software [3].
The gap state model for amorphous and polymorphous layers consists of two exponential tail states and two Gaussian distributions to simulate deep dangling bonds. The chosen parameters are consistent with previous experimental work [9]. The activation energy of a-Si:H(n) was taken equal to 0.2 eV. Considering the c-Si substrate, we fixed a lifetime of 1 ms (measured by µ-PCD), and a doping concentration of 8x10^{14}cm^{-3} deduced from the C-V measurements. The TCO reflectivity (average reflectivity 16.2%) spectrum was implemented in the front contact as well as the absorption measured by ellispometry (average absorption 7.5%). The interface defects were simulated by a 1 nm thick defect layer having a defect density of 10^{18} cm^{-3}. The front and rear surface recombination velocities were set equal to 10000 cm/s and 1000 cm/s, respectively, the latter corresponding to a conventional aluminium BSF (doping level 5.10^{18} cm^{-3}, depth 1µm). The study does not take into account the possible influence of the contacts. Figure 6 shows the simulated quantum efficiency (EQE, IQE) compared with the measurements made at ISE (CalLAB). Only the absorption spectrum had to be slightly modified to fit the experimental data. This can be explained by a possible variation in the TCO layer properties during the annealing step for the silver paste at 200°C.

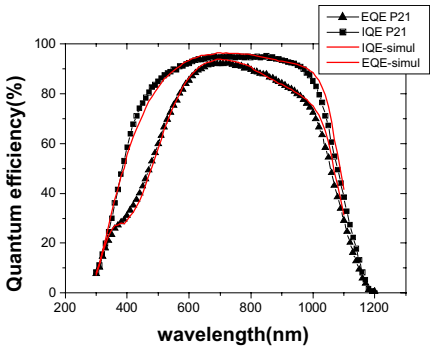

Fig.6: Validation of parameters for simulating the a-Si:H/pm-Si:H/c-Si solar cell P2I.

The first step is to understand the limitations of the open-circuit voltage of the a-Si:H/pm-Si:H/c-Si solar cells. A Vco of 613.4 mV with respect to 618 mV for the reference cell does not represent the real potential of the heterojunction. Figure 7 shows the effect of the interface defect state density on Voc. It appears that the interface quality is a strong limiting factor of Voc which indicates that the pm-Si:H/c-Si interface is still not fully optimised and requires further improvement. The difference measured in the short circuit current density Jsc between the heterojunction solar cell (31.2 mA/cm²) and the reference cell (32.4 mA/cm²) comes from many parameters. For example, the reflectivity as well as the absorption of the TCO layer are higher than for the SiN layer.

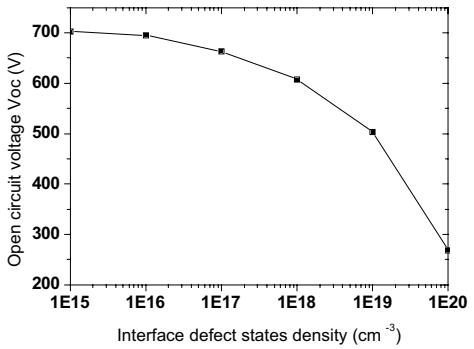

Fig.7:Influence of the pm-Si:H/c-Si interface defect density on the open-circuit voltage of the solar cell

From the IQE plot, a loss in the low wavelength range can be explained by the strong absorption of the deposited n-type amorphous emitter layer. As a consequence, the reduction of the emitter thickness through simulation leads to a higher Jsc value. Finally, Table II presents the possible improvements of a front a-Si:H/pm-Si:H/c-Si heterojunction using a textured surface for reducing reflection, as well as a thinner emitter (5 nm), an improved interface (defect density=$10^{17}cm^{-3}$), and a better front-printed contact quality (improved R_s=1Ω.cm²).

	Voc(mV)	Jsc(mA/cm²	FF(%)	η(%)
Experiment	613.4	31.2	70.0	13.50
Maximum	680.7	34.0	75.0	17.30

Table.II : Efficiency improvement of the a-Si:H/pm-Si:H/c-Si solar cell from simulation results

CONCLUSION and PERSPECTIVES

We have fabricated front a-Si:H/pm-Si:H/c-Si heterojunction solar cells on p-type silicon wafers and we achieved a maximum efficiency of 13.5% (ISE CalLAB) on 25 cm² areas. The whole process was performed at temperatures below 200°C except for the back contact treatment. The use of low temperature screen-printed polymeric/silver paste for the front contact on a TCO layer is possible and represents a real advantage to build solar cell on large areas. The relatively low fill factor of 70% was explained by a high resistivity of the printed fingers and needs to be improved in order to reach values higher than 75%. Capacitance-temperature measurements indicated that the surface state density at the pm-Si:H/c-Si interface is lower than $10^{12}cm^{-2}$. A simulation study using the AFORS-HET software aimed at analysing the limiting parameters and the possible improvements. The interface appears to be the main limiting factor of the Voc, while the current limitation mainly comes from the TCO layer. Also, a textured surface would lead to a reduction of the reflectivity. Furthermore, the reduction of the a-Si:H emitter thickness should improve the collection of photogenerated carriers in the low wavelength range. Taking into account all these potential improvements, a high Voc (640-680 mV), a Jsc value of 34 mA/cm², and an efficiency over 17% could be achieved on large area front side a-Si:H/pm-Si:H/c-Si heterojunction solar cells on p-type c-Si.

ACKNOWLEDGMENTS

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