BASIC ELECTRONIC PROPERTIES AND TECHNOLOGY OF TCO/a-Si:H(n)/c-Si(p) HETEROSTRUCTURE SOLAR CELLS: A GERMAN NETWORK PROJECT

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ABSTRACT: We report on a German network project in which the technology and the basic electronic properties of amorphous/crystalline silicon heterojunction solar cells are investigated. In contrast to the approach of Sanyo our focus is on hetero solar cells fabricated on p-type substrates without an a-Si:H(i) buffer-layer. One goal of the project is to transfer the results obtained on single crystalline wafers to inexpensive substrates, such as block-cast multicrystalline silicon or edge-defined film-fed grown silicon. All solar cells investigated here are completely processed at low temperatures (<250°C). Simulation studies show that a critical parameter is the defect density at the interface between the amorphous and the crystalline semiconductor both at the front and rear side. The interface state density has to be minimized to obtain maximum open circuit voltages. Using optimised deposition conditions of the amorphous silicon efficiencies larger 17% are obtaind on p-type c-Si wafers and larger 18% on n-type c-Si. For large area cells a low temperature screen printing process was developed. On a cell area of 10×10 cm² an efficiency of 12.9% on block-cast multicrystalline silicon is achieved.

Keywords: Heterojunction, Solar cell

1 INTRODUCTION

Heterojunction solar cells composed of hydrogenated amorphous silicon (a-Si:H) deposited on single crystalline silicon wafers (c-Si) gain more and more interest for high efficiency solar cells. Sanyo reported an efficiency larger 21% of for an a-Si:H(p, i)/c-Si(n)/a-Si:H(i, p) solar cell [1]. The high efficiencies were obtained by implementing an intrinsic a-Si:H layer between the doped a-Si:H layer and the c-Si wafer both at the front and at the rear surface. However, the efficiencies for heterojunction solar cells based on p-type substrates are still significantly lower than for solar cells based on n-type substrates.

Two main advantages arise from the a-Si:H/c-Si solar cell structure: i) The a-Si:H layer can be deposited at low temperatures (< 230°C). Any high temperature steps such as a back surface field diffusion can be omitted. This can be very important for temperature sensitive substrates such as thin film silicon on glass ii) Hydrogenated amorphous silicon is known to passivate silicon surfaces in an excellent way [2]. Thus, the a-Si:H/c-Si concept has the potential for high open circuit voltages.

In this paper the results of a German network project are described. In this project the technological and the scientific expertise of the partners is combined to develop highly efficient a-Si:H/c-Si heterojunction solar cells. In contrast to the approach of Sanyo the focus of the project is on a-Si:H(n)/c-Si(p) structures. All process steps of the solar cell fabrication should be performed at temperatures below 250°C. The results obtained on single crystal c-Si wafers are transferred to inexpensive substrates as block-cast multicrystalline (mc-Si) and edge-defined film-fed grown silicon (EFG-Si) wafers. Additionally, low temperature passivation schemes based on a microwave-induced remote-hydrogen plasma are evaluated to improve the bulk lifetime of these materials. Due to the low process temperatures any possible thermal lifetime degradation can be completely avoided. Industrially relevant processes like a low temperature screen-printing step are implemented and stability tests are performed. In addition to the technological approach one goal of the project is to improve the fundamental physical understanding of the a-Si:H/c-Si heterojunction. A sketch of the band diagram of an a-Si:H(n)/c-Si(p)/a-Si:H(p) structure is shown in Fig. 1. The heterojunction is dominated by two interfaces between a-Si:H and c-Si. Both interface are characterised by an interfaces state density, D_{it}, and band offsets, ΔE, which arise due to the different band gaps of a-Si:H and c-Si. The a-Si:H layer itself exhibits a high concentration of deep bulk defects and band-tail states.

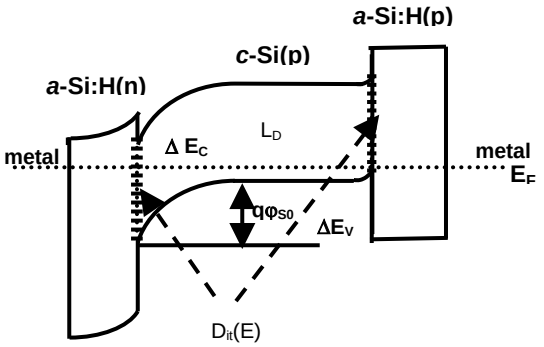

Fig. 1: Scetch of the band diagram of an a-Si:H(n)/c-Si(p)/a-Si:H(p) heterojuction solar cell.

2 EXPERIMENTAL

The silicon heterojunction solar cells were fabricated by deposition of hydrogenated amorphous silicon on c-Si wafers by plasma enhanced chemical vapour deposition (PECVD) or by electron cyclotron resonance CVD. Doping was achieved by mixing silane with phosphine and diborane for n-type and p-type doping, respectively. Prior to the a-Si:H deposition the wafers were cleaned by a RCA cleaning sequence and a HF-dip.

As transparent conductive oxide either ZnO or ITO were used. The contact grid at the front side was formed by evaporating Al or Cr/Ag. Definition of the contact grid was done by photolitography. An additional aim of the project is the development of a low temperature screen printed front contact grid for large area solar cells. On the rear side of the solar cells, Al was evaporated.

The simulations presented in this work were performed using the simulation program AFORS-HET [3].

3 RESULTS

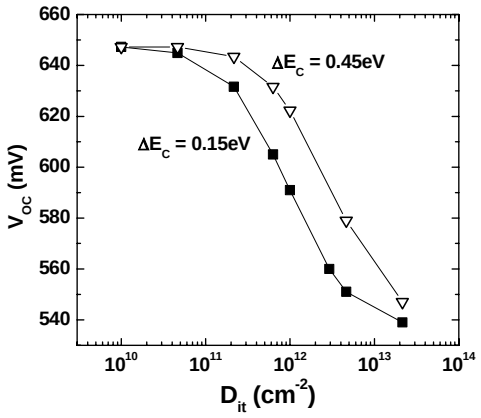

Fig. 2: Simulated open circuit voltage,V_{OC}, of an a-Si:H(n)/c-Si(p) solar cell as a function of the interface states density for two different values of the conduction band offset, ΔE_C.

As shown in Fig. 1, the a-Si:H/c-Si heterojunction solar cell is dominated by two interfaces between a-Si:H and c-Si. The interface is characterised by an interface states density and band offsets. Simulation results have indicated that a high interface defect density severely reduces the open circuit voltage [4]. To illustrate the effect Fig. 2 shows V_{OC} as a function of the interfaces states density for two different values of the conduction band offset for a Metal/a-Si:H(n)/c-Si(p)/Metal structure. For $D_{it} < 5\times10^{10}$ cm^{-2} Voc is nearly constant at about 647meV with increasing D_{it} for ΔE_C = 0.15eV. A further increase in D_{it} results in a significant decrease of Voc. Between $5\times10^{10}cm^{-2} < D_{it} < 5\times10^{12}$ cm^{-2} V_{OC} decreaes by about 90 meV from 640 to 550meV. The open triangles in Fig. 2 show the situation when the band offset for the minority carriers is large. In this case the decrease of V_{OC} with increasing D_{it} starts at $D_{it} \approx 3\times10^{11}cm^{-3}$. However, ΔE_C was determined to be about 0.15eV [5] and thus the solar cell is strongly influenced by D_{it} even at low values.

These results show that it is a major task for optimising the solar cell to reduce the interface states density. This can be done in several ways: i) The cleaning of the c-Si wafers can be optimised in such a way that the growth of the a-Si:H results in a low D_{it}. ii) The deposition conditions can be set that an optimal growth of the a-Si:H is achieved. iii) A passivation layer between the doped a-Si:H and the c-Si can be implemented. Sanyo reported that the insertion of an intrinisic a-Si:H layer leads to a significant enhancement of V_{OC} due to a well passivated c-Si surface. However, this was shown for solar cells based on n-type substrates only. Fig. 3 shows IQE spectra of an a-Si:H(n, i)/c-Si(p) heterojunction solar cell with different a-Si:H(i) layer thicknesses, $d_{a\text{-}Si:H(i)}$. In this solar cells a boron diffused back surface field was implemented. A thin a-Si:H(i) layer (3nm) leads to an enhancement of the IQE in the short wavlength region compared to the sample which contains no intrinsic layer. A further increase in the a-Si:H(i) layer thickness leads to a reduction in the IQE. This is due to internal losses in the emitter. Previously it was published that the emitter thickness leading to maximum effieciency is at about 5 nm [6].

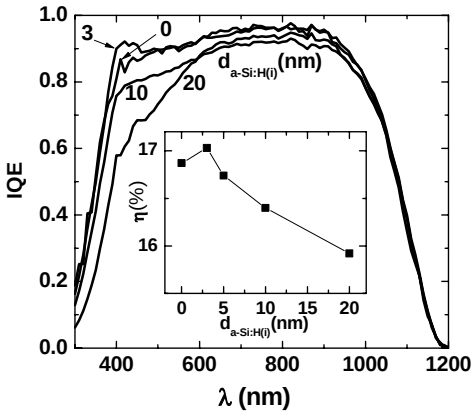

Fig. 3: Internal quantum efficiency of an a-Si:H(n, i)/c-Si(p)/BSF solar cell with different a-Si:H(i) layer thickness. The inset shows the corresponding efficiencies.

The inset in Fig. 3 shows the efficiency of the solar cells as a function of the a-Si:H(i) layer thickness. For $d_{a\text{-}Si:H(i)}$= 0 nm an efficiency of 16.9% was achieved. This value is slightly increased to 17.1% for $d_{a\text{-}Si:H(i)}$= 3 nm and decreases for thicker a-Si:H(i) layers. This finding is supported by the results of the IQE measurements. When the a-Si:H layer becomes thicker internal losses in the defect rich layer causes a reduction in the IQE and thus in the efficiency. In contratst to results reported from Sanyo for an a-Si:H(p, i)/c-Si(n) solar cell the insertion of an a-Si:H(i) layer in an a-Si:H(n)/c-Si(p) structure only leads to marginal device improvement. This can have several reasons: i) the defect density of the a-Si:H(i) layer is still too high and thus the passivation effect is not improved compared to an a-Si:H(n) layer, ii) the band allignment becomes unfavourable by inserting the a-Si:H(i) layer. Further investigations are necessary. The interface states density can also be optimized by the a-Si:H deposition conditions. Fig. 4 shows the solar cell efficiency of an a-Si:H(n)/c-Si(p) heterojunction solar cell with a diffused back surface field as a function of the deposition temperature of the a-Si:H layer. Clearly a maximum of η = 16.9% can be observed for $T_S \approx 230°C$.

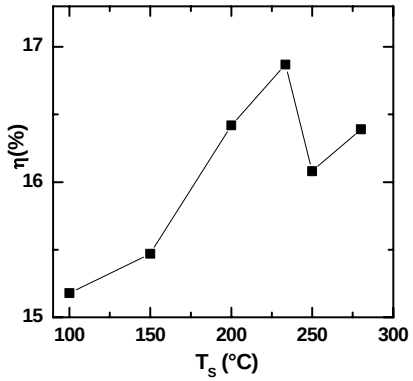

Fig. 4: Efficiency of an a-Si:H(n)/c-Si(p)/BSF solar cell as a function of the deposition temperature of the a-Si:H.

These results are consistent with photoluminescence results which show that the photoluminescence intensity is highest around this temperature and thus the interface recombination rate is lowest [7].

The rear side of the solar cell structure is an important part of the device. Figure 5 shows V_{OC} values determined by simulation of an a-Si:H(n)/c-Si(p) heterojunction with varying surface recombination velocity at the rear side. For S > 10 cm/s, V_{OC} decreaes rapidly from about 677mV to 647 mV at S = 10^4cm/s. In the project different kinds of low temperature processed rear sides were compared. Table I summarises V_{OC} data obtained for an a-Si:H(n)/c-Si(p) heterojunction solar cell with different rear side concepts. Serving as a reference a boron-diffused rear side results in a V_{OC} of 635mV. Using an a-Si:H(p) layer with a thickness of about 35nm a V_{OC} of about 634mV was obtained. In contrast to the diffused rear side the a-Si:H(p) coated rear side is processed at temperartures below 230°C. Additionally, a COSIMA rear side was implemented which results in a comparable V_{OC} as the former two structures. The COSIMA rear side uses the passivation effect of a-Si:H combined with local Al contacts evaporated on top of the a-Si:H layer. This structure is annealed at low temperature to form the contact of Al to the base of the cell [8]. Recently the University of Stuttgart developed a rear side consisting of a stack of a-Si:H(i), a-Si:H(p), µc-Si(p) and ZnO. Using a diffused emitter as a front electrode a V_{OC} of 678mV was achieved resulting in a

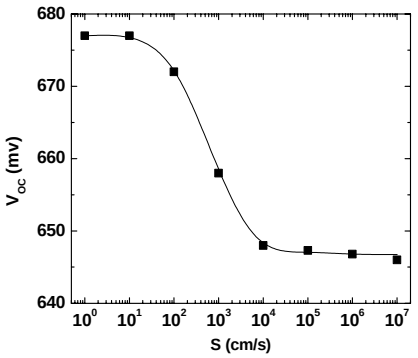

Fig. 5: Simulated V_{OC} as a function of the rear side recombination velocity for an a-Si:H(n)/c-Si(p) solar cell.

Rear side	Front side	Voc(mV)
Diffused	a-Si:H(n)	635
a-Si:H(p)	a-Si:H(n)	634
COSIMA	a-Si:H(n)	629
a-Si:H(i, p)/µc-Si(p)/TCO	Diffused	678

Tab. I: Open circuit voltages for solar cell structures with different rear contacts.

confirmed efficiency of the device of 21% [9]. This is a promising result for low-temperature a-Si:H back contacts on p-type Si wafers. This back contact will be implemented in a complete a-Si:H/c-Si solar cell structure in the next future. Note that all developed rear contact systems are in accordance with our low temperature approach.

The quality of the passivation of the c-Si surfaces and the quality of the substrate can be investigated by luminescence measurements [10]. The quasi Fermi level splitting which is determined by quantitative photoluminescence measurements gives the maximum achievable V_{OC}. Fig. 6 shows calibrated luminescence spectra of a c-Si wafer after different process steps in the processing of an a-Si:H/c-Si solar cell structure. The splitting of the quasi Fermi levels can be deduced from the formula of the rate of spontaneous emission fitted to the calibrated photoluminescence spectra [11]. Each step of the solar cell production increases the maximum achievable V_{OC} up to V_{OC} = 667mV.

As mentioned above, one goal of the network project is the transfer of the results obtained for single crystalline silicon to cheaper substrates such as mc-Si and EFG-Si. The diffusion lengths in these materials are usually

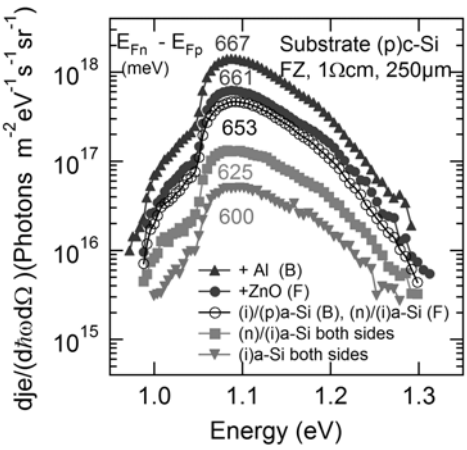

Fig. 6: Measured calibrated luminescence spectra of a-Si:H/c-Si heterostructures. The numbers gives the maximum achievable open circuit voltages.

smaller than diffusion lengths meausred in float-zone and Czochralski-grown single crystalline silicon wafers. To obtain high solar cell efficiencies, the diffusion length should be well above the wafer thickness. For many multicrystalline silicon wafer materials this is not initially the case. To improve the carrier lifetime of the mc-Si or EFG-Si materials, a phosphorus gettering step is performed in the typical commercial solar cell processes. This phoshporus diffusion step at ~870°C creates the n^+ emitter and effectively removes metallic contaminants from the material. The diffusion is followed by a

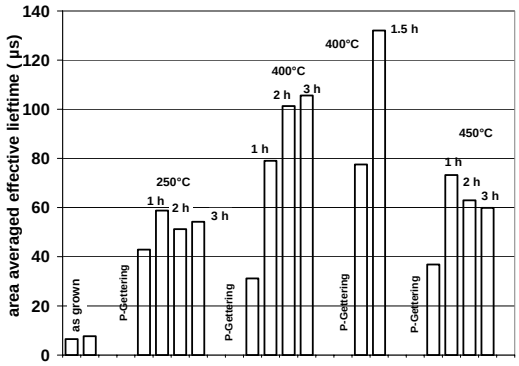

Fig. 7: Effective lifetime of EFG-wafers averaged over an area of 25cm². After a P-gettering step the wafers were exposured to a remote H-plasma for different temperatures and times.

hydrogenation step, which is usually combined with the contact firing at high tempertures (~800°C). During the firing, hydrogen diffuses from the a-SiNx:H layer deposited at the front into the bulk where it passivated defects, leading to a further increase in lifetime. A low-temperture alternative to the latter step is the H-passivation using microwave-induced remote-plasma hydrogen treatment. In Fig. 7, the effective lifetime of several neighbouring EFG-Si wafers averaged over an area of 25 cm² is shown for different passivation times and temperatures. Prior to the H-passivation, a P gettering step was performed.. The averaged lifetime of the as-grown EFG-Si is only 6 µs. This value is strongly enhanced by a P-gettering step up to a factor of ~10. H-passivation leads to a further pronounced increase in the lifeime. The lifetime depends strongly on the plasma-hydrogenation temperature. The highest lifetimes are obtained for a hydrogenation temperature of 400°C and a passivation time larger 1 h. The averaged lifetime of about 130 µs is comparable to the lifetime obtained using the high-temperature SiN-hydrogenation treatment. The H-passivation by microwave-induced remote-plasma hydrogenation can be easily implemented in a production line and is in accordance with the low-temperature approach of the heterojunction solar cell concept.

One goal of the project is to develop and investigate industrially relevant processes. Therefore, a low-temperature screen printed front contact was implemented. The grid is optimized for a sheet resistivity

Structure	Area (cm²)	Eta
a-Si:H(n)/c-Si(p)/a-Si:H(p)	1	17.1
a-Si:H(p)/c-Si(n)/a-Si:H(n)	1	18.2
a-Si:H(n)/c-Si(p)/BSF	10×10	15.0
a-Si:H(n)/mc-Si(p)	10×10	12.9
a-Si:H(n)/EFG-Si(p)/a-Si:H(p)	8×8	12.7

Tab.II: Efficiencies of different heterojunction solar cell processed in the network project.

of the TCO which is about 50 Ω/sq. The commercially available silver polymer screen-printing paste is modified by some additives to obtain an optimized contact finger structure. The temperature during the screen printing is always lower than 230°C. More details can be found in Ref. 12.

Table II summarizes the efficiencies obtained so far on p-type and n-type substrates for small (1cm²) and large (8x8cm²) area solar cells. All solar cells were processed at temperatures below 230°C. The large area solar cells on mc-Si and EFG-Si were processed with the low temperature screen printed front contact. The solar cells were performed without an additional a-Si:H(i) layer.

Stability tests performed on a-Si:H/c-Si solar cells using ITO as the TCO and an Cr/Ag front grid showed no degradation of the solar cell parameters. Details can be found in Ref. 13.

CONCLUSION

In conclusion, the combined work of the network project lead to efficient a-Si:H/c-Si solar cells on single crystal and inexpensive substrates. To process the solar cells completely at low temperatures different rear sides have been tested. Promising candidate is a stack of a-Si:H and µc-Si for a good passivation as well for a good contact to the rear electrode. For the front contact a low temperature screen printing was developed. Additionally to the technological approach a detailed physical knowledge has been gained during the project.

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