DESIGN CRITERIA FOR AMORPHOUS/CRYSTALLINE SILICON HETEROJUNCTION SOLAR CELLS, - A SIMULATION STUDY

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ABSTRACT

Amorphous/crystalline silicon heterojunction solar cells, TCO/a-Si:H(n)/c-Si(p), are investigated by means of numerical computer simulation. The influence of (1) the a-Si:H(n) emitter thickness, (2) the defect density of the emitter/wafer interface and (3) the TCO/emitter front contact system on the solar cell-performance is studied and compared with experimental results. The use of an intrinsic a-Si:H(i) buffer layer and of a p-doped a-Si:H(p) back surface field layer is addressed, modelling TCO/a-Si:H(n)/a-Si:H(i)/c-Si(p)/a-Si:H(p) solar cell structures. Some general design criteria for a-Si:H/c-Si heterojunction solar cells are derived, suggesting an optimum emitter thickness for a given (measured) front contact TCO/emitter built-in potential.

1. INTRODUCTION

Solar cell devices, based on amorphous/crystalline silicon heterojunctions (a-Si:H/c-Si) have raised considerable interest. Thin film a-Si:H layers are deposited by plasma enhanced chemical vapor deposition on both sides of a high-quality c-Si wafer, thus realising the solar cell emitter and the back surface field (BSF-layer) of the solar cell. Due to the comparatively low conductivity of doped a-Si:H, the further use of a transparent, conductive layer (TCO) on top of the a-Si:H emitter is required. The high potential of such a technology has been recently demonstrated by Sanyo reaching 20.7 % cell efficiency in the laboratory and 15% for a commercial module [1]. While in Japan the work concentrates on using n-type c-Si wafers, the work in Europe mainly uses p-type c-Si wafers predominantly. To our knowledge, so far the highest efficiency of 16.2 % on a p-type c-Si wafer has been obtained on a flat, unstructured FZ-Si <111> substrate [2].

The performance of these kind of solar cells not only critically depends on the a-Si:H-emitter thickness, but also on the properties of the three additional interfaces: (1) emitter/wafer interface, (2) TCO/emitter interface, and (3) wafer/BSF-layer interface. The cell properties can be varied by changing the quality and type of the thin film silicon material used [3], by incorporation of an undoped a-Si:H(i) buffer layer, and by using either n- or p- type c-Si wafer material [4].

By means of modelling and numerical computer simulation, the influence of an intrinsic a-Si:H(i) buffer layer, of the TCO/emitter front contact and of a BSF-layer on the solar cell performance (efficiency, open-circuit voltage, short-circuit current, fill factor and internal quantum efficiency) is investigated for p-type wafer material. It is the aim of this work to improve the understanding of this device and to derive arguments for design optimisation.

2. MODELLING

We used AFORS-HET for solving the one dimensional semiconductor equations based on Shockley-Read Hall recombination statistics. AFORS-HET is a simulation tool, which was developed in our group and will be distributed for public use [5]. For the individual semiconducting layers, as well as for the interfaces between them, particular defect state distributions have to be specified.

Considering the crystalline c-Si(p) absorber, a doping concentration of $N_a = 1.5\ 10^{16} cm^{-3}$ and a constant defect state distribution of $D = 10^{11} cm^{-3}\, eV^{-1}$ throughout the bandgap was assumed. This corresponds to a high quality FZ wafer (1 Ωcm) with a minority carrier diffusion length of $L_e = 500\,\mu m$, a value which is larger than the wafer thickness of 300 µm.

For the amorphous silicon layers, a-Si(n), a-Si(i) and a-Si(p) a band gap of $E_g = 1.72\,eV$ and an electron affinity of $\chi = 3.8\,eV$ was assumed. For the doped films the doping concentration was set to $N_d = 10^{19} cm^{-3}$. The defect-state distributions within the band gap are exponential band tail states and Gaussian dangling bond states. The corresponding data is taken from literature [6,7], adapted to our own measurements [8], and sketched in Fig. 1. The parameters result in an activation energy $E_A=E_C-E_F$ of $E_A = 0.25\,eV$ in case of n-doped a-Si(n), $E_A = 0.82\,eV$ in case of intrinsic a-Si(i) and $E_A = 1.32\,eV$ in case of p-doped a-Si(p).

For modeling the a-Si/c-Si interface, a constant defect state distribution D_{it} [cm^{-2} eV] throughout the c-Si bandgap is assumed, leading to an integrated total interface state density N_{it} [cm^{-2}]. If there is an intrinsic buffer layer, the thickness of the intrinsic layer is assumed to be equal to the thickness of the doped layer. The TCO front contact is modeled by specifying the TCO/emitter surface recombination velocity S_{front} and the TCO/emitter built-in potential $q\phi_{front}$. A built-in potential of $q\phi_{front} = 0\,eV$ corresponds to no additional band bending (flat-band condition) due to the front contact, $q\phi_{front} > 0$ corresponds to a depletion of the emitter. A measured reflection and absorption loss of the incident solar AM1.5 radiation crossing the 80 nm thick TCO front contact has been incorporated, as shown in Fig. 2b.

All results shown in this paper have been calculated for flat, untextured substrates in order to be able to compare these simulations to our own experimental results [2,9], which led to cell efficiencies in the 16 % region. Using in addition a BSF-layer and surface texturing, the simulated solar cell efficiencies exceed 20 %.

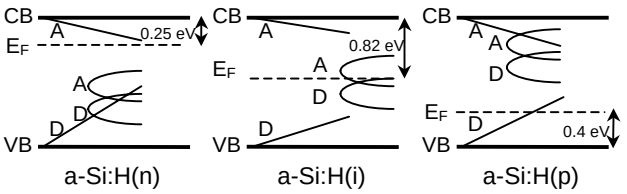

Fig. 1: Sketch of the acceptor-like (A) and donor-like (D) defect-state distributions within the bandgap, Eg = 1.72 V, of a-Si:H(n), a-Si:H(i) and a-Si:H(p), used in the simulation.

3. INFLUENCE OF THE EMITTER THICKNESS

In a first approximation we neglected defect states at the emitter/wafer interface and the influence of the TCO/emitter front contact (flatband condition).

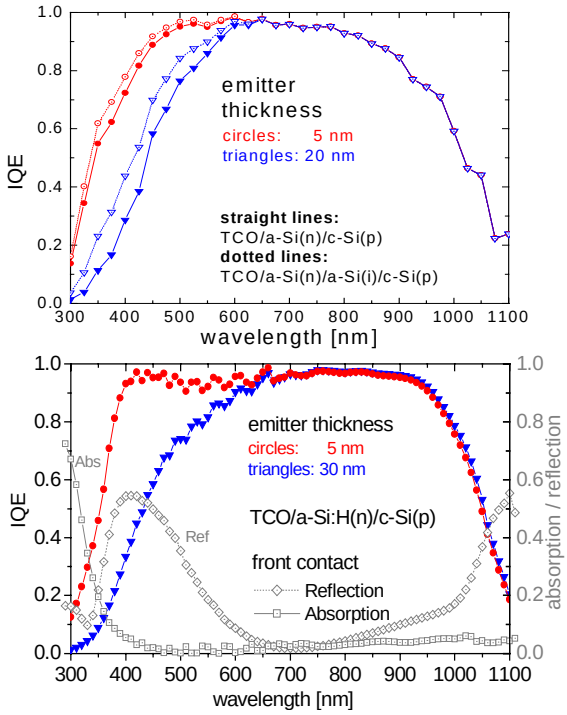

Fig. 2: (a) Simulated and (b) measured internal quantum efficiency of a-Si:H(n)/c-Si(p) heterojunction solar cells. Parameter is the thickness d of the emitter layer. Also shown is the measured absorption and reflection loss of the 80 nm thick TCO front contact, which was incorporated in all simulations.

The simulated results of Fig.2 and Fig.3 suggest to keep the a-Si:H emitter as thin as technologically possible: Since a-Si:H is much more defective than c-Si, most carriers generated in the emitter recombine. The diffusion length of holes in the emitter is in the range of a few nm only. A thinner emitter will therefore enhance the internal quantum efficiency in the short wavelength region (300 nm to 650 nm), where emitter absorption is significant (Fig.2). This enhancement of IQE with decreasing d is due to two effects: With decreasing d the absorption within the defect-rich emitter will be reduced and a larger portion of the minority carriers can cross the heterojunction. For d = 5 nm, the IQE at low wavelengths (< 350 mn) is restricted due to the TCO absorption and no longer due to the a-Si:H emitter.

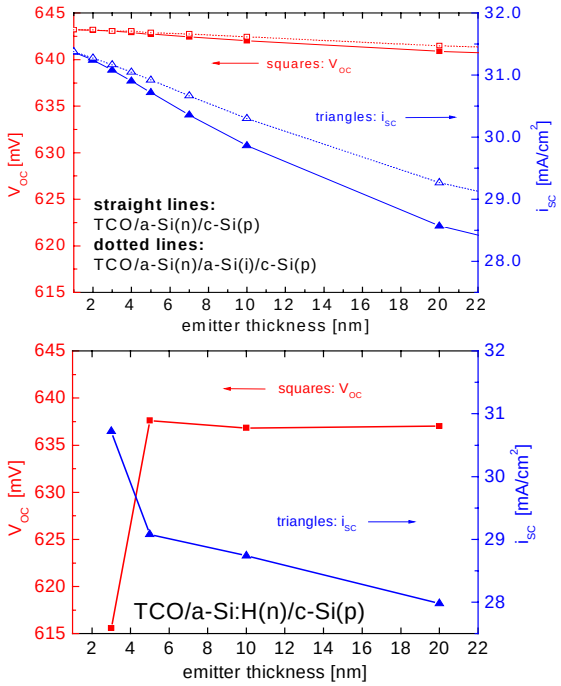

Fig. 3: (a) Simulated and (b) measured short-circuit current density i_{SC} and open-circuit voltage V_{OC} as a function of the emitter thickness d.

These findings are in agreement with the behavior of j_{SC} and V_{OC} shown in Fig.3. With decreasing d the short-circuit current is strongly enhanced while the V_{OC} is influenced only little. The experimental data follow these trends down to d = 5 nm. For smaller d of 3 nm, however, there is a sudden drop in V_{OC} of 23 mV. There is experimental believe, that this is not due to pinholes within the ultrathin emitter layer [5], as a 5 nm thick a-Si(n)/a-Si(i) emitter also shows this drop in V_{OC}, see table 1. We attribute this experimentally observed voltage drop to a non-negligible TCO/a-Si:H built-in potential $q\phi_{front}$. So, for ultrathin emitters, the properties of the TCO/emitter front contact can no longer be neglected. The simulations shown in Fig.5.a (chapter 6) suggest that indeed carrier depletion within the thin a-Si:H layer due to the TCO/a-Si:H(n) contact will result in such voltage drops.

Furthermore, the measured open-circuit voltage is lower than expected from the simulation (638 mV instead of 643 mV). We assign this difference to the non-negligible TCO/a-Si:H built-in potential $q\phi_{front}$ and to the influence of interface states at the emitter/wafer interface.

4. INFLUENCE OF AN INTRINSIC BUFFER LAYER

Comparing a-Si:H(n) and a-Si:H(n)/a-Si:H(i) emitters of the same total thickness, experimentally, an increase of V_{OC} with the introduction of a buffer layer is observed, if the emitter layer is thick enough (10 nm, Table 1). However, for a thinner emitter, there is a decrease of V_{OC} (5 nm, Table 1). This behavior is not observed in the simulation if one neglects the influence of the emitter/wafer and of the TCO/emitter interface.

The increase in V_{OC} is attributed to a better defect passivation of the emitter/wafer interface, using intrinsic a-Si:H(i) instead of doped a-Si:H(n), compare Fig.4, chapter 5. The decrease in V_{OC} is attributed to the non-negligible TCO/a-Si:H built-in potential $q\phi_{front}$, compare Fig. 5a, chapter 6.

cell structure	Voc [mV]
80nm TCO / 10nm a-Si:H(n) / c-Si(p)	638
80nm TCO / 5nm a-Si:H(n) / 5nm a-Si:H(i) / c-Si(p)	642
80nm TCO / 5nm a-Si:H(n) / c-Si(p)	638
80nm TCO / 2.5nm a-Si:H(n) / 2.5nm a-Si:H(i) / c-Si(p)	600

Table 1: Experimental V_{OC} of a-Si:H/c-Si heterojunction solar cells with different emitters.

According to the simulation, we find that the inclusion of a buffer layer results in an enhancement of i_{SC}, if one again compares emitters of the same total thickness, and neglects defects at the emitter/wafer interface (see Fig.3.a). As already discussed, for ultra thin emitter layers, the emitter is not electrically dead. As a-Si:H(i) is less defective compared to a-Si(n), more holes created within the buffer layer will be collected. Thus the blue response of the internal quantum efficiency is enhanced (see Fig.2.a). However, the main effect of the intrinsic buffer layer is to ensure a better emitter/wafer interface passivation.

5. INFLUENCE OF THE EMITTER/WAFER INTERFACE

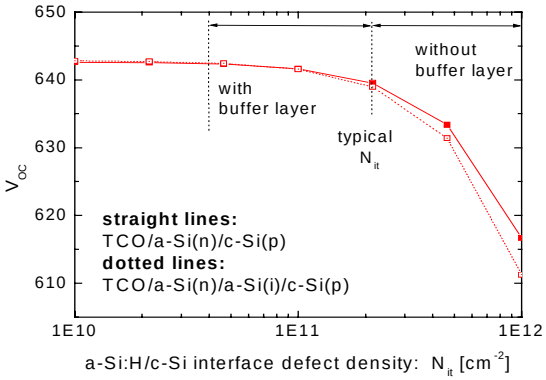

Fig. 4: Simulated dependence of the open-circuit voltage on the emitter/wafer interface state density, with and without using an intrinsic buffer layer. The emitter thickness is 10 nm, the influence of the TCO/emitter contact has been neglected (flat-band conditions).

So far interface states at the emitter/wafer interface have been neglected. Such states will significantly reduce the open-circuit voltage of the solar cell (Fig.4). The reduction in open-circuit voltage is due to additional interface recombination and can be partially suppressed by ensuring a strong band bending in the crystalline absorber [4]. According to Fig.4, the total concentration of interface defects should be less than $N_{it} \approx 10^{11}$ cm^{-2}. This appears possible making use of the excellent surface passivation that can be achieved with intrinsic a-Si:H(i) [10]. Using an intrinsic a-Si:H(i) buffer layer, there are probably less defects at the a-Si:H/c-Si interface, which leads to the increase in open-circuit voltage mentioned above.

6. INFLUENCE OF THE TCO/EMITTER FRONT CONTACT

The front contact TCO/a-Si:H(n) built-in potential $q\phi_{front}$ is expected to be somewhere in the range 0.2 – 0.4 eV [3,11]. As a result of this, the TCO/emitter front contact will drive the a-Si:H(n) emitter into depletion. Taking the TCO/emitter front contact into consideration, for $q\phi_{front} \geq 0.3$ eV there is now a significant decrease in open-circuit voltage, if the a-Si:H emitter gets too thin (Fig.5). The critical emitter thickness at which the decrease in V_{OC} starts, is larger if an intrinsic a-Si:H(i) buffer layer is used (Fig.5). With a negligible front contact built-in potential, $0 \leq q\phi_{front} \leq 0.2$ eV, V_{OC} increases slightly with decreasing d, independent from the emitter type (Fig.5 and Fig.3a).

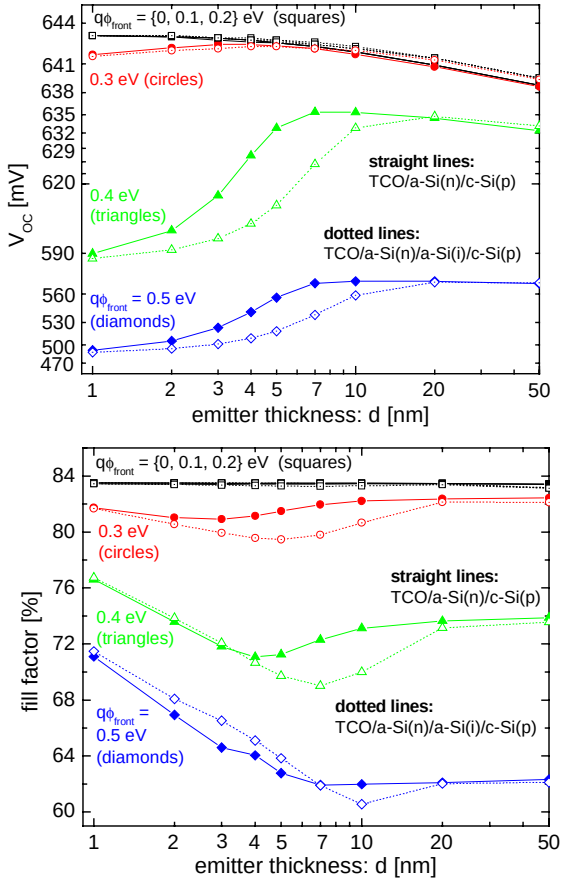

Fig. 5: Simulated (a) V_{OC} and (b) fill factor of a-Si:H/c-Si heterojunction solar cells with or without a buffer layer as a function of the emitter thickness d. The parameter is the TCO/emitter built-in potential $q\phi_{front}$.

A non-negligible front contact TCO/emitter built-in potential can thus explain the experimentally observed decrease of V_{OC} for thin emitter layers, mentioned in chapter 3 and chapter 4. In the measured thickness dependence of V_{OC} in Fig.3b, there is a voltage drop of 23 mV, as the emitter gets thinner than 5 nm. For a 5 nm thick emitter, the use of an intrinsic buffer layer leads to a voltage drop of 38 mV, like stated in table 1. According to the results of the simulations shown above, this corresponds to a front contact TCO/a-Si:H(n) built-in potential somewhere between 0.3 - 0.4 eV.

In order to shield the electric field imposed by the front contact built-in potential, the depletion zone within the a-Si:H emitter would be approximately 10 nm thick. If the emitter gets thinner than 10 nm, additional carriers from the absorber and recharged defects from the emitter have to be used to shield the electric field. This considerably alters the band bending in the crystalline absorber and leads to a strong decrease of the fill factor and of V_{OC} (Fig.5a and b) [3]. The critical emitter thickness, at which this decrease starts, is larger when an intrinsic buffer layer is used, because in this case there are less carriers from the emitter available in order to shield the electric field.

There exists now an optimum emitter thickness, depending on the front contact TCO/a-Si:H(n) built-in potential and on the type of the emitter used. As long as $q\phi_{front} \leq 0.2$ eV, the influence of the TCO/emitter front contact is negligible and the emitter should be deposited as thin as technologically possible. For 0.3 eV $\leq q\phi_{front} \leq$ 0.4 eV, the optimum emitter thickness is about 5-7 nm (no buffer layer) and 10-15 nm (with buffer layer) respectively.

7. INFLUENCE OF THE BSF-LAYER

So far, no interface passivation at the back side of the solar cell has been assumed ($S_{back} = 10^7$ cm/s), in analogy to the solar cells processed. In order to reach higher efficiencies, excellent interface passivation at the back contact and light trapping due to surface texturing is necessary.

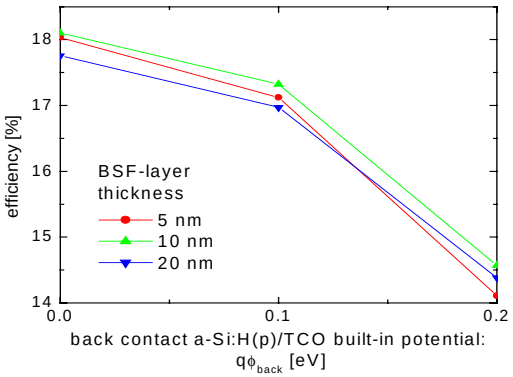

Fig. 6: Influence of an a-Si:H(p) BSF-layer on the solar cell performance of a-Si:H/c-Si heterojunction solar cells. Simulated solar cell efficiency as a function of the back contact a-Si:H(p)/TCO built-in potential $q\phi_{back}$. The parameter is the thickness of the BSF-layer.

Using a p-doped a-Si:H(p) back-surface field (BSF) layer, and assuming a sufficient interface passivation (interface trap density smaller than 10^{11} cm^{-2}), the open-circuit voltage can be enhanced by 30 mV, from 643 mV to 673 mV, and the corresponding solar cell efficiency will rise from 16.5 % to 18.1 % (Fig.6). In this simulation no light trapping due to texturing has been taken into account. The influence of the thickness of the BSF-layer on the solar energy performance is not as critical as compared to the emitter layer. However, the influence of the back contact a-Si:H(p)/TCO built-in potential $q\phi_{back}$ is much more severe, see Fig.6. One has to ensure that $q\phi_{back} \leq 0.1$ eV, in order to enhance the solar cell efficiency.

8. CONCLUSION

Some general design criteria for amorphous/crystalline silicon heterojunction solar cells have been found: *(I) Ensure a good a-Si:H/c-Si interface passivation* (optimum value: $N_{it} \leq 10^{11}$ cm^{-2}). If the incorporation of an intrinsic a-Si:H(i) buffer layer enhances V_{OC} for thick emitters it should be used, otherwise it should be omitted. *(II) Measure and minimize the front contact TCO/a-Si(n) built-in potential* (optimum value: $q\Phi_{front} \leq 0.2$ V, however this value will probably be higher, i.e. 0.3 V $\leq q\Phi_{front} \leq$ 0.4 V). *(III) Minimise the emitter thickness to an extent that the band bending of the crystalline absorber at the emitter/wafer interface is not lost*. This critically depends on the front contact TCO/emitter built-in potential $q\phi_{front}$ and of the type of emitter used. For $q\phi_{front} = 0.3$ eV the optimum emitter thickness is roughly 10 or 5 nm, using or not using an intrinsic buffer layer. For a lower/higher $q\phi_{front}$ the optimum emitter thickness is lower/higher. If $q\phi_{front} \leq 0.2$ eV, the emitter should be deposited as thin as technologically possible. *(IV) An a-Si:H(p) BSF-layer is only helpful if the back contact a-Si:H(p)/TCO built-in potential is small, i.e. $q\phi_{back} \leq 0.1$ eV.*

Acknowledgement

This work was partially supported by the German Department of Education and Research (BMBF), contract #01SF0016.

References

[1] H.Sakata, T.Nakai, T.Baba, M.Taguchi, S.Tsuge, K. Uchihashi, S.Kiyama, *Proc. 20th IEEE PVSEC* (2000), 7.

[2] M.Scherff, A.Froitzheim, A.Ulyashin, M.Schmidt, W.Fahrner, W.Fuhs, *Proc. PV in Europe, Rome, Italy, Oct. 2002*, 216.

[3] R.Stangl, A.Froitzheim, W.Fuhs, *Proc. PV in Europe, Rome, Italy, Oct. 2002*, 123.

[4] R.Stangl, A.Froitzheim, L.Elstner, W.Fuhs, *Proc. 17th Eur. PV. Sol. En., Munich, Germany, Oct. 2001*, 1387.

[5] A.Froitzheim, R.Stangl, M.Kriegel, L.Elstner, W.Fuhs, *this conference (WCPEC-3, Osaka, Japan, May 2003).*

[6] R.Schropp, M.Zeman**, a-Si and µc-Si Solar Cells**, *Kluwer Acad. Publishers* (1998), 183.

[7] H.Stiebig, F.Siebke, Philos. Mag. B (UK), **72**, 1995, 499

[8] M.Schmidt, A.Schoepke, O.Milch, T.Lussky, W.Fuhs, Mat.Res.Soc.Symp.Proc., **762**, 2003, A.19.11.1.

[9] A.Froitzheim, M.Scherff, A.Ulyashin, M.Schmidt, W.Fahrner, W.Fuhs, *this conference (WCPEC-3, Osaka, Japan, May 2003).*

[10] S.Dauwe, J.Schmidt, R.Hetzel, *Proc. of 25th IEEE PVSEC Conf., New Orleans, USA, May 2002.*

[11] M.Schmidt, A.Froitzheim, R.Stangl, L.Elstner, K.Kliefoth, W.Füssel, W.Fuhs, *Proc 17th EUR PVSEC, Munich, Germany, Oct.2001.*