INTERFACE PROPERTIES OF a-Si:H/c-Si HETEROJUNCTIONS INVESTIGATED BY ADMITTANCE SPECTROSCOPY

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ABSTRACT: Admittance properties of a-Si:H(n)/c-Si(p) heterostructures with a-Si:H(n) emitter layers of different thickness and with different a-Si(n)/c-Si(p) interface characteristics were studied both from experimental results and from a numerical modelling. The temperature dependence of the capacitance generally exhibits two steps, accompanied with two bumps in the conductance, which are shifted to higher temperatures for increasing frequencies. The first step occuring in the low temperature range (100 K – 200 K) is attributed to the activation of the transport in the a-Si:H layer and depends on the layer thickness and Fermi level position in a-Si:H. The second step is caused by trapping–detrapping of charge carriers at interface states and occurs at higher temperature (> 200 K) when the interface defect density at the a-Si:H/c-Si interface (D_{int}) exceeds 10^{12} cm^{-2}. The presence, position and amplitude of the high temperature step can be used for a-Si:H/c-Si interface characterization and are discussed in the light of numerical modelling results.
Keywords: Heterojunction, interfaces, silicon.

1 INTRODUCTION

Hydrogenated amorphous/crystalline silicon heterojunctions, a-Si:H/c-Si, are of great interest for high efficiency solar cells fabricated in a low temperature process. The efficiency of such solar cells may reach up to 21% [1] and the usage of low temperature a-Si:H deposition instead of high temperature diffusion process for the fabrication of the junction emitter makes them attractive for low cost photovoltaic applications. However, the efficiency of such devices mainly depends on the resulting a-Si:H/c-Si interface properties, i.e. on the c-Si surface pre-treatment and the deposition parameters of the a-Si:H layer. Thus interface characterisation methods are very important to understand interface properties and to find out the best surface pre-treatment and a-Si:H growth conditions and thickness. We here present the results of the interface properties investigation using admittance spectroscopy. Comparison of the modelling results with experimental data allows us to determine and verify the effect of the a-Si:H layer parameters and of the defect density at the a-Si:H/c-Si interface on admittance properties.

2 EXPERIMENTS

A series of heterostructures, TCO/a-Si:H(n)/c-Si(p)/Al, with a-Si:H(n) emitter layers of different thickness, and with different a-Si(n)/c-Si(p) interface treatments (using a thermal oxide or an HF dip prior to the emitter deposition), were fabricated by PECVD deposition of a thin phosphorous-doped a-Si:H(n) emitter layer on top of a p-type crystalline silicon wafer (FZ, 1 Ω cm). All preparation details are described in Ref. [2]. Contact to the a-Si:H emitter was made by a 80 nm thick ZnO(Al) layer deposited by sputtering. Evaporated aluminum was used to form a small grid onto the front contact and as the rear contact. Table 1 summarizes the thickness and wafer treatment of the studied structures.

The structures were characterized by capacitance and conductance versus temperature and frequency measurements (C-T-ω and G-T-ω), and capacitance versus voltage measurements (C-V). The admittance measurements were performed in a liquid nitrogen cryostat in the temperature range 93 K – 333 K using a HP4284A impedance meter at frequencies in the range 20 Hz – 1 MHz.

Table 1: Wafer pre-treatment and n-type a-Si:H layer thickness for samples under study.

Sample	Wafer pre-treatment	n-type a-Si:H layer thickness (nm)
1	Tunnel oxide	40
2	HF-dip	40
3	HF-dip	<10

3 SIMULATION DETAILS

The modelling of the heterostructures admittance and its dependence on temperature, frequency and bias was made using AFORS-HET, Version 1.1, a numerical PC program developed at HMI [3]. Using Shockley-Read-Hall recombination statistics, the one-dimensional semiconductor equations were solved for small sinusoidal modulations of the external applied voltage. Two series of numerical calculations were performed:

(i) The simple model of a-Si:H/c-Si heterojunction with two ohmic contacts and without interface states was solved for different a-Si:H layer thicknesses. The material parameters of the c-Si and a-Si:H layers are given in table 2. The value of the conduction band offset (0.15 eV from the electron affinities) and the distribution of the density of states in a-Si:H was taken according to photoyield experiments [4].

Table 2: Main parameters of heterojunction layers used in calculation

Parameter	c-Si	a-Si:H
Band gap, eV	1.12	1.74
Doping density, cm^{-3}	$1.5x10^{16}$	10^{20}
Electron affinity, eV	4.05	3.9

(ii) An additional defective thin layer (5 nm) was introduced at the interface, wherein the defect density was varied. The distribution of this defect density was taken to be independent on the energy.

4 RESULTS

Experimental plots of the capacitance per unit area, C, and of the conductance per unit area divided by the angular frequency, G/ω, are shown as a function of temperature at different frequencies in Fig 1. The main difference between samples comes from the presence or not of steps in the capacitance accompanied with bumps in the conductance in the low temperature range (100 K – 200 K). Both the capacitance steps and the conductance maxima are shifted to higher temperatures with increasing frequencies. This shift in the temperature versus frequency was used to obtain the activation energy of the underlying process, which is found to be approximately 0.2 eV. Depending on the wafer treatment, we observe either one or two capacitance steps in the capacitance versus temperature (C-T) curve, that are accompanied by one or two peaks in the conductance versus temperature (G-T) curve. For the sample with the HF dip treatment and a-Si:H thickness below 10 nm, no capacitance step at all could be observed [5].

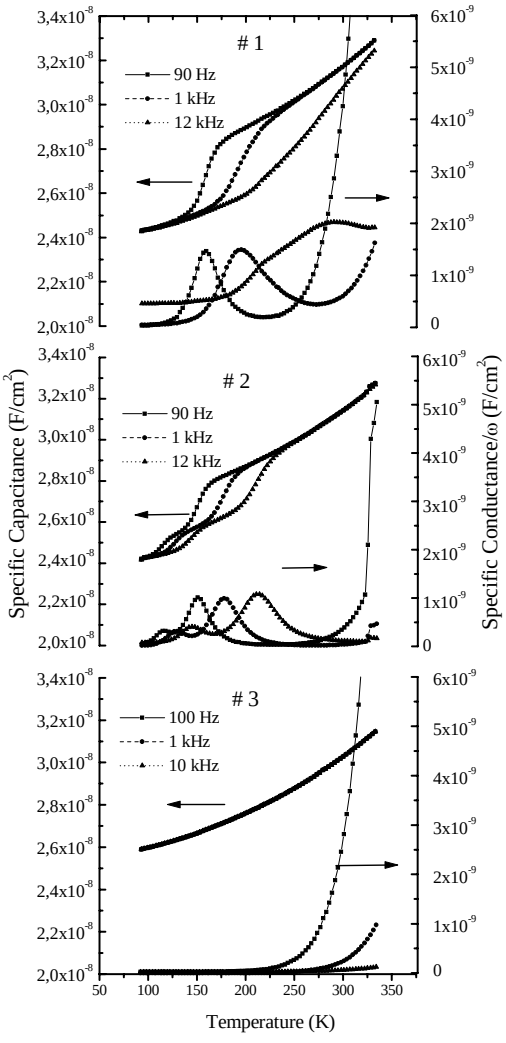

Fig. 1. C-T-ω and G/ω-T-ω curves for the samples #1, #2 and #3.

The plots of the inverse square capacitance versus bias voltage are presented in Fig. 2. They have a well defined linear behavior with only a very small deviation at low reverse bias. The linear behavior means that C-V curves are determined by the depletion region in crystalline silicon. The doping density of c-Si wafers obtained from the slope of the plots ($1.2 \pm 0.1 \times 10^{16}$ cm^{-3}) is in agreement with the wafer resistivity. The intercept of these plots with the bias axis yields the total potential drop across the junction, referred as the diffusion potential. As can be seen from Fig. 2, we obtain a value of 1V at 300 K for all the samples.

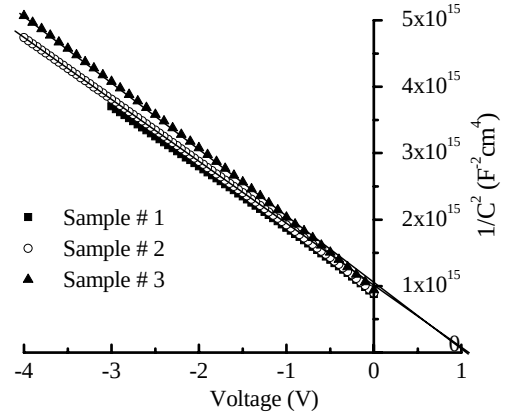

Fig. 2. Experimental C-V characteristics of the samples at 1 kHz and at 300 K.

The results of numerical simulations of C-T-ω and G-T-ω curves for the first case without interface defects for different a-Si:H thickness are shown in Fig. 3. The absolute value level of the calculated capacitance is slightly higher than experimentally due to the slightly higher doping density of the c-Si. For the case of 40 nm emitter thickness, one step in the capacitance occuring between 100 and 200 K depending on the frequency can be clearly seen. This step is also accompanied by a peak in the conductance. The activation energy obtained from the temperature and frequency dependence of the peak maximum is equal to 0.29 eV. By decreasing the a-Si:H layer thickness the amplitudes of the capacitance step and conductance peak decrease. For 5 nm a-Si:H thickness the capacitance step becomes almost invisible and the absolute value of the conductance peak is very small.

The second series of simulations was made for 40 nm thick a-Si:H layer with different interface defect density. Simulated C-T-ω and G-T-ω curves with D_{int} varying from 10^{10} to 2×10^{13} cm^{-2} are presented in Fig. 4 and Fig 5, respectively. For D_{int} varying from 0 to 10^{10} cm^{-2} no difference in the C-T-ω and G-T-ω curves were observed. When D_{int} increases to 10^{12} cm^{-2} a slight rise of the capacitance value was observed without any deviation of the dependence on temperature and frequency. While D_{int} reaches 4×10^{12} cm^{-2} the capacitance level significantly increases and a second capacitance step appears at higher temperature (200-250K), accompanied by a second conductance peak, as shown in Fig 5. An activation energy of 0.46 eV can be

deduced from these second features . Finally, for D_{int} equal to 2×10^{13} cm^{-2} the capacitance level further drastically increases and the second step becomes significantly larger and shifted to higher temperature (250-300K).

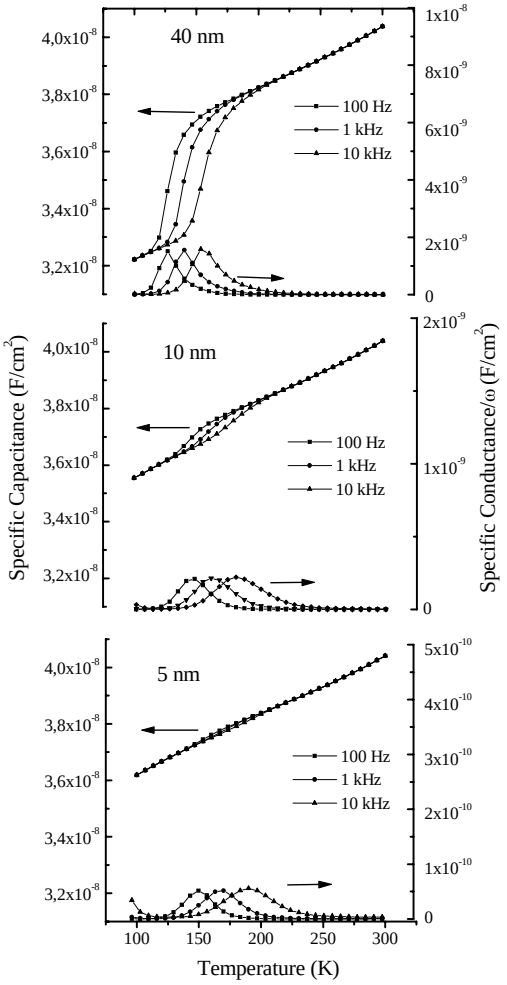

Fig. 3. Calculated C-T-ω and G-T-ω curves for a-Si:H thickness of 40, 10 and 5 nm, and no interface defects.

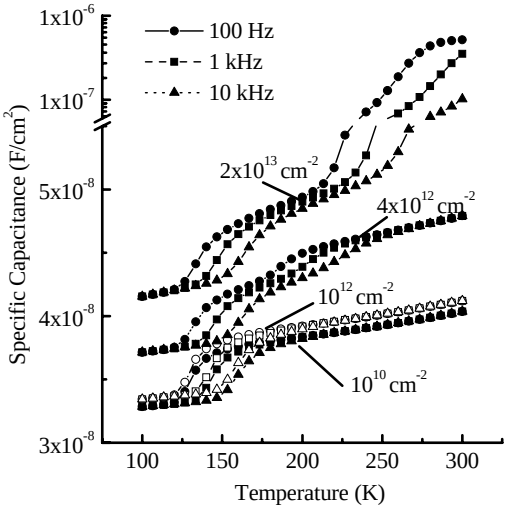

Fig.4. Calculated C-T-ω curves for D_{int} 10^{10}, 10^{12} (open symbols) $4x10^{12}$ and $2x10^{13}$ cm^{-2}. The a-Si:H layer thickness is 40 nm.

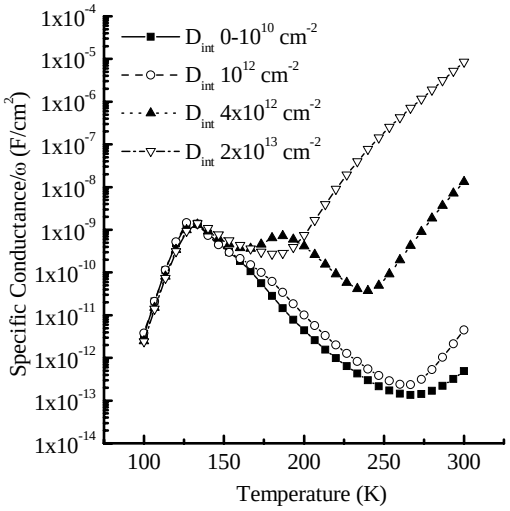

Fig.5. Calculated G-T-ω curves at 100 Hz for different D_{int} .

For the same values of D_{int} the bias dependence of the capacitance was also calculated. The plots of the inverse square capacitance versus bias voltage are shown in Fig. 6. For D_{int} from 0 to 10^{12} cm^{-2} the plots are linear and almost identical. For D_{int} equal to 4×10^{12} cm^{-2} the plot is still linear but slightly shifted due to the increase of the c-Si capacitance resulting from the decrease of the space charge width in c-Si. With further increasing D_{int} up to 2×10^{13} cm^{-2} a strong deviation from linearity of the plot takes place at low reverse voltage. This effect is frequency dependent as can be seen in Fig. 4. The intercept of the $1/C^2$-V plots with the voltage axis are independent on interface states for D_{int} lower than 10^{12} cm^{-2} and give the value of diffusion potential equal to 0.77 eV, which corresponds to the expected value considering the position of the Fermi level in both a-Si:H and c-Si and conduction band offset introduced in the simulation.

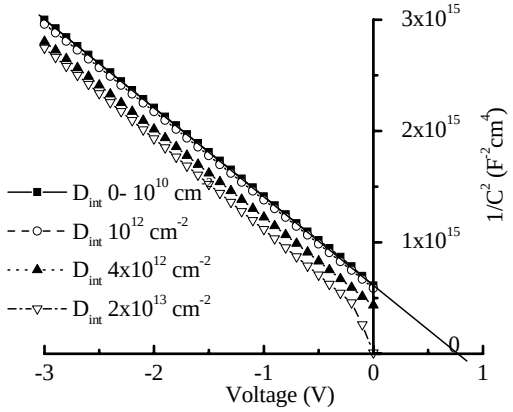

Fig. 5. Calculated C-V characteristics for different D_{int}.

5 DISCUSSION

The presence of the step in the C-T-ω curve at low temperature is attributed to the onset of the transport or of the response of gap states at the Fermi level in the a-Si:H emitter. At very low temperatures, below the step, the capacitance per unit area is given by $\varepsilon/(d+w_c)$, where ε is the silicon dielectric permittivity, d is the a-Si:H thickness and w_c is the width of the depletion layer in c-Si. Above the onset, the capacitance changes to $\varepsilon A/(l_{eff}+w_c)$, determined by the sum of the depletion region w_c in c-Si and the effective depletion length l_{eff} in a-Si:H. The activation energy of this process corresponds to the difference between the bottom of the conduction band and the Fermi level in a-Si:H if the statistical shift of the Fermi level in a-Si:H can be neglected.

The increase of the capacitance level with the increase of D_{int} is explained by the fact that when D_{int} exceeds 10^{12} cm^{-2} it leads to a decrease of band bending in c-Si and therefore of the depletion region width. So, this can be considered as an indirect consequence of the increase of D_{int}. On the opposite, the high temperature step is caused by trapping and emission of charge carriers at interface states, which are directly related to D_{int}. As can be seen in Fig. 3, C-T-ω and G-T-ω measurements are not sensitive to D_{int} values below 10^{12} cm^{-2}. Similar conclusions were already inferred from numerical modelling of the frequency dependence of the heterostructure capacitance [6].

Comparing the experimental data in Fig. 1 we can conclude that the fabricated heterojunctions have D_{int} values less than 10^{12} cm^{-2}. In that case interface defects do not affect the C-V characteristics. So, in principal using the intercept method of the $1/C^2$ versus V plot should allow to determine the conduction band offset between a-Si:H and c-Si. However, it should be mentioned that the admittance of the solar cell may be also affected by the TCO/a-Si:H contact. In Ref. 7, it was shown that the ZnO/a-Si:H contact may have a barrier height of 0.3-0.4 eV. The precise influence of this top contact on the admittance deserves further investigations.

6 CONCLUSION

Experiments and numerical modelling have shown that several different features can be observed in the C-T-ω and G-T-ω plots: steps of the capacitance accompanied with bumps in the conductance in the low temperature range (100 K – 200 K), or at high temperature (> 200 K). The first step is related to the transport in a-Si:H layer and depends on the a-Si:H thickness. The high temperature step is caused by carrier exchanges with interface states and appears when D_{int} exceeds 10^{12} cm^{-2}. Therefore it can be used for a rough estimation of the interface quality.

Acknowledgment
This work was partly supported by ADEME (Agence de l'Environnement et de la Maîtrise de l'Énergie)

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