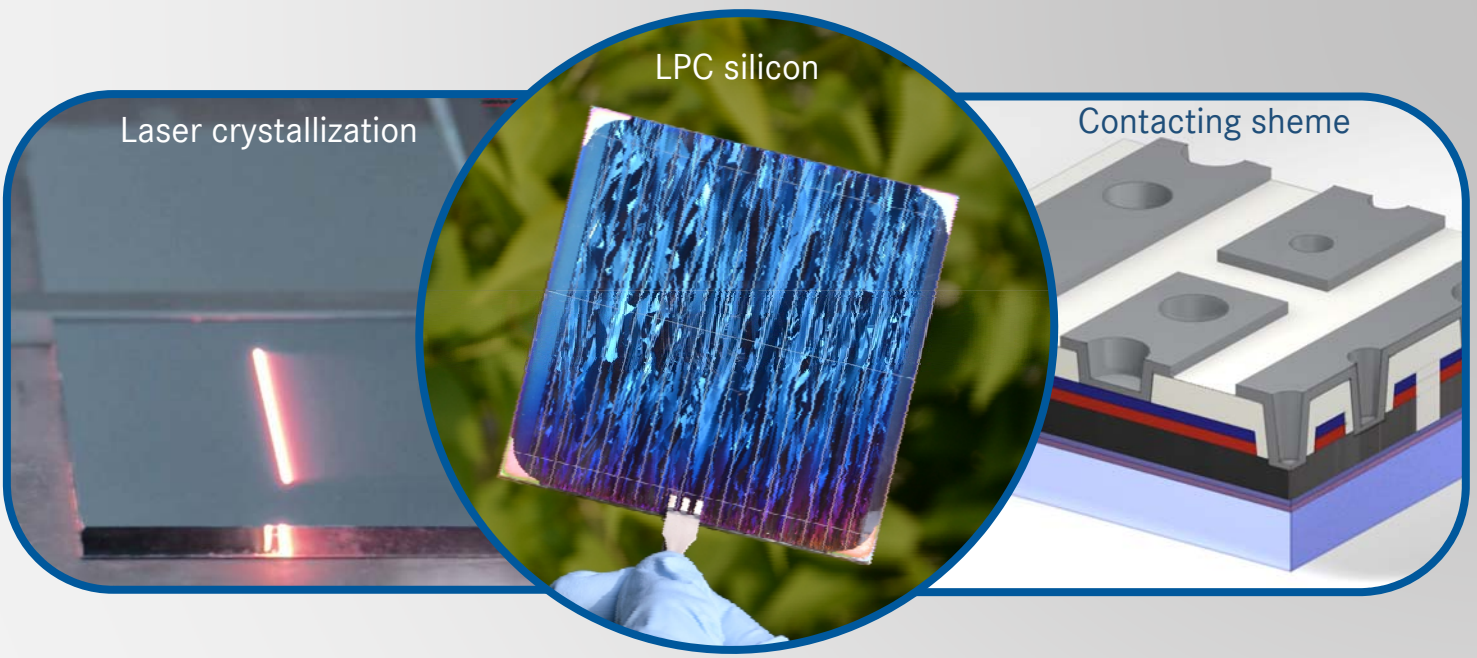
Liquid **P**hase **C**rystallized Silicon on Foreign Substrates (**LPC**)

LPC-technology could combine the best of both worlds, the high material quality of wafer based silicon with the low material consumption and the low cost, large area processing capability of thin film technologies. Moreover layer thicknesses are freely selectable to suit the demands of the required application without handling issues due to a direct processing on foreign substrates.



LPC-Technology

The liquid phase crystallization technology (LPC) of silicon on foreign substrates was developed in a joint research of the Technical University Hamburg-Harburg and the Helmholtz-Zentrum Berlin für Materialien und Energie (HZB) in 2011. As an advanced zone melting process, LPC-technology utilizes state of the art laser systems to fabricate high quality multi-crystalline silicon layers directly on foreign substrates. Prior to laser crystallization sophisticated multilayer pre-cursor stacks are prepared with our high-end deposition tools. With the help of the single sided contacting schemes developed at HZB exciting opportunities open up for a variety of applications such photovoltaics, silicon on insulator (SOI) applications, sensors or displays on rigid or flexible substrates.

Application: Example PV

At HZB we are able to process the resulting layers in an industrial-compatible process to interdigitated back contacted (IBC) solar cells and modules. Despite the few number of institutions that have explored this new and exciting technology in terms of PV, the great expectations were fully met in the shortest possible time, as the learning curve of figure 1 impressively demonstrates.

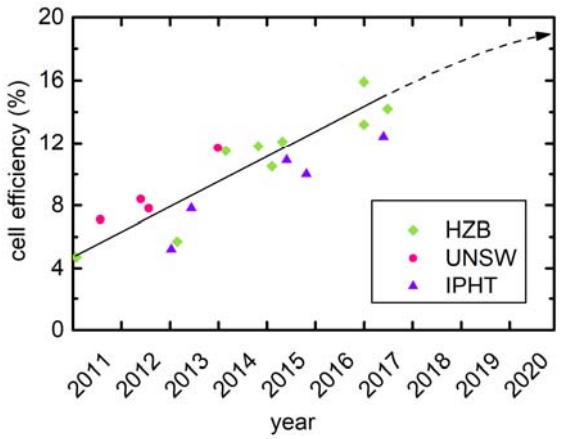


Figure 1: Learning curve of the LPC-technology

The LPC-technology developed at HZB has what it takes to fulfill the demands of the next generation photovoltaic application. We are convinced to continue our progress approaching the efficiency of multi-crystalline silicon wafers.

Development and patent situation

Based on its know-how of the full manufacturing process HZB provides lab scale LPC prototypes. HZB holds 3 granted (plus 10 pending) IP families.

DE 10 2014 105319 B4
DE 20 2013 011997 U1
DE 10 2011 111629 B4

Material Facts

- **thin film processing**
  - ⇨ thicknesses of 0.2 µm ≤ x ≤ 60 µm
  - ⇨ standard: 10 – 15 µm
- **large grains**
  - ⇨ several mm × cm (width × length)
- **high purity**
  - ⇨ O/N/C below CESI standard
- **excellent electrical properties**
  - ⇨ open circuit voltage: V_{OC} ≤ 661 mV
  - ⇨ intra-grain mobility: µ ~ 100 % c-Si
  - ⇨ inter-grain mobility: µ ~ 90 % c-Si
  - ⇨ surface recombination: s ≤ 300 cm/s
  - ⇨ minority carrier lifetime: τ > 5 µs

Process Facts

- **low material consumption**
- **scalable to large areas**
- **interdigitated back contact (IBC) cell and module technology**
- **wafer-like silicon quality**

Contact

LPC-Team

Department
Silicon Photovoltaics

☎ +49 30 8062 41330
✉ LPC-Team@helmholtz-berlin.de