A Dilemma: Dielectrics for Wide-Bandgap Gallium Oxide High-Voltage Transistors

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Abstract

As the wide-bandgap semiconductor Gallium Oxide matures for high-voltage transistors, the lack of p-type doping requires field-effect transistors. That brings into sharp limelight the need for new dielectrics. We have recently realized gallium oxide vertical field-effect transistors with >1 kV breakdown for the first time. The voltage switching capability in these transistors is limited not by the semiconductor, but by the dielectrics.

1. Introduction

Because of the availability of large area single crystal substrates and the large bandgap of ~4.5 eV, beta-Gallium Oxide offers the potential for high-voltage electronic devices that could potentially surpass the performance of GaN and SiC, which have bandgaps of ~3.4 eV. For the particular application of high-voltage diodes and transistors, if the larger breakdown electric fields due to the large bandgap could be exploited, there is hope for realistic applications, in spite of several material limitations.

Today, there are four primary limitations of Gallium Oxide for high voltage electronic switches. The **first** is its low thermal conductivity, which will limit the amount of electrical energy it can handle without heating up to a point it degrades or becomes unstable. The **second** is that the electron mobility is not as high as in bulk GaN or SiC, which limits the speed and energy efficiency with which the high voltage switching can be performed. The **third** is that no p-type acceptor dopant has been found for beta Gallium Oxide yet, which implies the lack of p-n junctions, which in turn implies that the intrinsic breakdown voltages of this material cannot be exploited yet, as it is done in SiC, and more recently in GaN.

The lack of p-type Gallium Oxide implies one must use Schottky or Field-effect gates for transistors. The maximum voltages handled by Schottky gates are limited by Fowler-Nordheim tunneling determined exponentially by the Schottky barrier height, which is typically ~1-2 eV, falling far short of the entire bandgap of Gallium Oxide, and making the resulting transistor not attractive for high voltages. This leads to the need for high quality dielectrics, and M-I-S gates that can prevent the Fowler-Nordheim tunneling and improve the breakdown voltage. And that leads to the **fourth** problem, and the subject of this work. The dielectrics that have been successful for Silicon, SiC, and GaN are simply not enough as they limit the potential of Gallium Oxide, as we have recently found in our experimental demonstration of the first kV-class Gallium Oxide transistors.

2. Experimental

Fig 1 shows the first kilovolt-breakdown Gallium Oxide vertical transistors that we have realized and reported recently [1]. Lateral channel transistors, be it MESFETs, or HEMTs, cannot deliver the current handling capacity and high-voltage simultaneously because of the mobility limits of Gallium Oxide, and are limited less by the semiconductor channel, and more by the surface and dielectrics. Vertical devices allow for far superior field termination, and current drives. Because we do not have a p-type Gallium Oxide, the device shown in Figure 1 uses a ~330 nm wide fin with vertical sidewalls with very low background n-type doping in the channel. Then, a 30 nm Al_2O_3 dielectric is deposited conformally on the sidewalls by ALD, followed by a 50 nm sputtered Cr sidewall metal. The source contact is made to a heavily n-type doped Gallium Oxide layer on the top, and the drain is on the back side of the wafer. The electron current thus follows vertically down from the source to the drain and is modulated by field-effect from the sidewall gates through the ALD dielectric. This device geometry in principle is no different from a double-gated lateral FET turned on its side, but in practice it offers for far higher breakdown voltages because of the geometry.

3. Results and Discussion

Figure 2 shows the transfer characteristics of the transistor. The transistor is enhancement mode and normally off as is desired for high-voltage switches. It shows a high on/off ratio, which limited by the gate leakage current as can be seen in Figure 2. The 30 nm gate dielectric on the sidewalls "does the job", but is not ideal, and can be improved substantially in the future. For example, we observe a hysteresis of <0.2 Volt, and potentially the presence of interface traps that reduce the electron mobility in the channel in addition to the shift in the threshold voltage. It is not yet clear yet if the sidewall etch causes the introduction of traps in addition to those that are at the ALD interface. We

are evaluating the interfaces with several pulsed measurements, and hope to extract further information of this interface in due time.

Figure 3 shows the three-terminal breakdown voltage at a gate voltage of 0 V. The breakdown exceeds 1kV, and is due to the gate current. From device modeling and visible investigation of device damage, we determine that the breakdown is definitely not due the Gallium Oxide, and not even primarily near the device shown in Fig 1, but outside near the gate pads. By proper edge termination and improvement of the gate dielectrics, or with new gate dielectrics, we expect to achieve higher breakdown voltages in Gallium Oxide transistors in the near future.

4. Conclusion

A dilemma of finding good dielectrics for ultra wide-bandgap semiconductors such as Gallium Oxide is highlighted in Fig 4. Because the bandgap of Gallium Oxide is so large, it encroaches into the regime of dielectrics themselves. For example, the bandgap of Al2O3 is hardly <2 eV more than the semiconductor, and the conduction band offset is even smaller, implying a rather small potential barrier. Crystalline Al_2O_3 may be the most attractive moving forward, but is very difficult to realize! We conclude that to exploit what Gallium Oxide has to offer, it is imperative that new classes of dielectrics with higher bandgaps and high dielectric constants are necessary.

References

[1] Z. Hu et al., IEEE EDL, (2018).

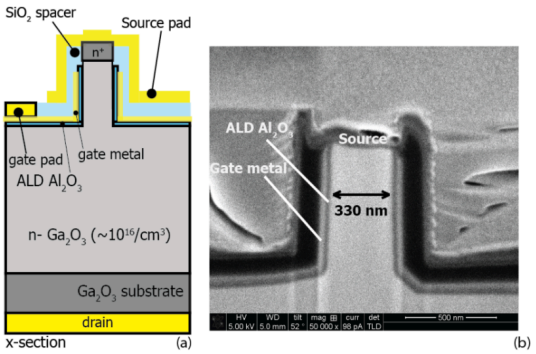

Fig.1: Vertical Gallium Oxide Transistor cross-section image and an SEM image of the fully processed device.

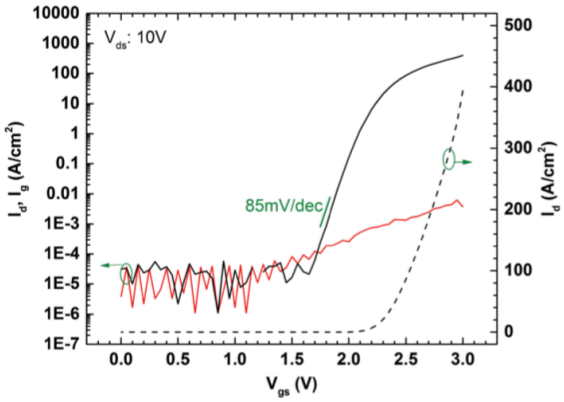

Fig.2: The vertical Gallium Oxide FET exhibits current saturation, E-mode operation, on/off ratios of 8 orders of magnitude, and a subthreshold slope is ~85 mV/decade.

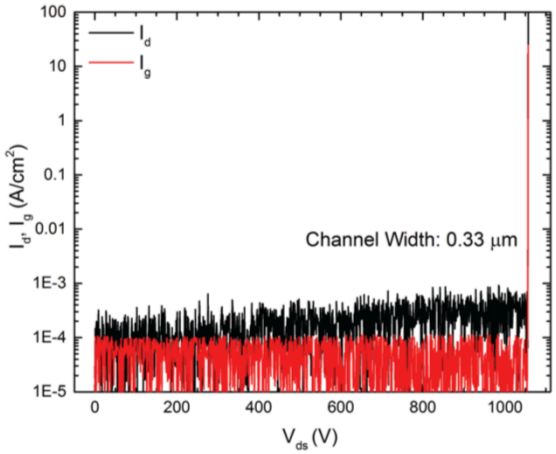

Fig.3: A breakdown voltage of >1000 V is measured in the vertical Gallium Oxide transistor.

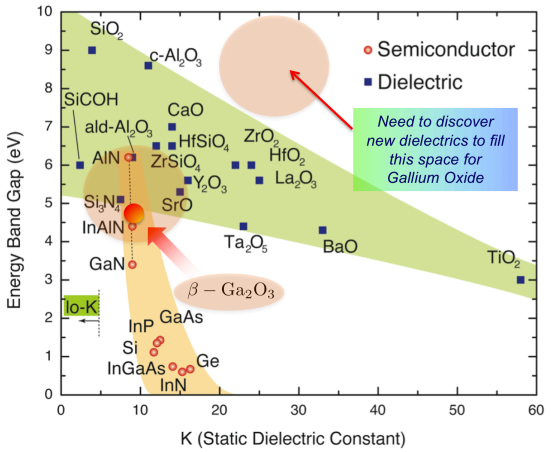

Fig.4: Because of the small band offset of a-Al_2O_3 with Ga_2O_3, it is not the ideal dielectric. SiO_2 offers superior band offsets, but has a low-K and therefore low gain. To exploit the potential of Ga_2O_3, new dielectric materials are needed.