STRUCTURAL AND ELECTRICAL PROPERTIES OF EPITAXIAL SI LAYERS PREPARED BY E-BEAM EVAPORATION

P. Dogan*, F. Fenske, L.-P. Scheller, K. Y. Lee, B. Gorka, B. Rau, E. Conrad, S. Gall, B. Rech
Hahn-Meitner-Institut Berlin
Kekuléstr. 5, 12489 Berlin, Germany
* Phone/Fax: +49-30-8062-1392/1333, E-mail: pinar.dogan@hmi.de

ABSTRACT: In this paper, structural and electrical properties of thin p-type Si films which are homoepitaxially grown at low substrate temperatures (T_s= 450-700 °C) with deposition rates of r_{Si}= 40-475 nm/min are discussed. Applying defect etching, films grown on Si(111) wafers exhibit a decreasing etch pit density with increasing T_s, and with decreasing r_{Si}. The defect etching of the films grown on poly-Si seed layers reveal regions of quite different crystalline quality with different underlying crystallographic orientations. The hole mobility of about 195 cm^2/Vs has been measured for the films grown on Si(100) wafers. The temperature dependent Hall mobility measurements have shown that the extended defects do not influence the hole mobility. Solar cells have been prepared on both Si(100) wafers and poly-Si seed layers. For this investigation, an open circuit voltage of 570 mV for wafer-based and 346 mV for glass-based solar cells have been reached.
Keywords: Low temperature Si epitaxy, crystalline Si, extended defects.

1 INTRODUCTION

Large-grained polycrystalline silicon (poly-Si) on glass is a promising material for efficient low-cost crystalline Si thin-film solar cells. One approach to realise such solar cells is based on the epitaxial thickening of a poly-Si seed layer (template) prepared by Aluminum Induced Crystallisation (AIC) of a-Si. [1]. Due to the thermal requirements of the glass substrate, the epitaxial growth needs to be applied with low thermal budget processes. Epitaxial thickening of a seed layer at such low temperatures was obtained by Electron Cyclotron Resonance Chemical Vapour Deposition (ECRCVD) [2], Ion Assisted Deposition (IAD) [3], Layered Laser Crystallization (LLC) [4], Hot-Wire CVD (HWCVD) [5], and Electron-Beam Evaporation [6].

This paper deals with the investigation of epitaxially grown Si films prepared by e-beam evaporation under non-ultra high vacuum conditions, without using a post-ionization stage as applied by the IAD method. In our previous work, using different crystallographic substrate orientations the influence of the substrate temperature (T_s) in the range of 550-650 °C on the film properties has been presented [7]. In this work, the influence of the deposition parameters T_s in the range of 450-700 °C and Si deposition rate (r_{Si}) have been investigated.

2 EXPERIMENTAL DETAILS

As substrates, monocrystalline Si(100) and Si(111) wafers ("ideal seed layers") and poly-Si seed layers on 0.7 mm thick Borofloat® 33 glass substrates have been used. The poly-Si seed layers have been prepared by using the AIC process, resulting in about 200 nm thick p^+-type poly-Si layers [8]. The substrates have been cleaned by a standard RCA procedure and immediately prior to loading into the load-lock of the deposition system treated with 2% HF for 30 s. No in-situ cleaning has been applied. The Si layers were grown by evaporating float zone quality material with an e-gun at rates of r_{Si}= 40-475 nm/min to a film thickness of 1.5-2 µm. The p-type doping was realized by co-evaporation of boron from an effusion cell. The base pressure was in the range of 10^{-6} Pa and the residual gas pressure during deposition was around 10^{-4} Pa. The substrates were held at ground potential.

For the extended defect analysis, the films have been investigated by a Scanning Electron Microscopy (SEM) after defect etching. The films were Secco etched for 10 s [9], whereas only some of the films grown on the poly-Si seed layers were Schimmel etched for 7 s [10]. Schimmel etching is more aggressive than Secco etching. Therefore, the same number and size of defects can be revealed in a shorter time. The grain orientation distribution was obtained by Electron Backscatter Diffraction (EBSD).

Temperature dependent Hall effect measurements were performed in the range of 20-300 K. The boron doped layers were grown on highly resistive (>3 kΩcm) n-type Si(100) wafers.

Two types of solar cells have been prepared: (a) wafer-based using a p^+-Si(100) wafer (2mΩcm) and (b) glass-based using a p^+-type poly-Si seed layer on glass. On these substrates the following layer sequence was deposited: epitaxially grown p-type Si absorber (1500-2000 nm) / n^+-type a-Si:H emitter (10 nm) / TCO (80 nm ZnO:Al) / Al contacts. The hetero-emitter was realized by a highly phosphorous doped a-Si:H layer deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) [11]. The ZnO:Al films were deposited by sputtering. The post-deposition treatments were applied directly after the absorber layer growth and consisted first of a Rapid Thermal Annealing (RTA) step at 850 °C for 100 s under nitrogen atmosphere and second of a hydrogen plasma passivation at 520 °C for 10 minutes using a plasma power density of 0.1 W/cm^2 [12,13].

The total area of the solar cells was 4 mm x 4mm. For wafer-based solar cells mesa contacting scheme and for glass-based solar cells interdigitated contacting scheme have been applied. The active areas were 10.65 mm^2, and 7.44 mm^2, respectively (used for solar cell measurements). The solar cells were characterized by current-voltage measurements at room temperature under illumination at 100 mW/cm^2 AM 1.5G irradiation. For the measurement of the glass-based solar cells white paper was used as a back reflector.

3 RESULTS AND DISCUSSION

3.1 Structural Properties

The influence of T_s in the range of 450-700 °C on the homoepitaxial growth on Si(111) and Si(100) wafers has been analysed. The deposition rate was 60-75 nm/min. Applying Secco etching, the films grown on Si(100) wafers exhibit for the whole temperature range investigated almost no etch pits, which are characteristic for extended defects. In contrast, the films grown on Si(111) wafers exhibit a significantly higher density of extended defects [7].The results are illustrated in Figure 1.

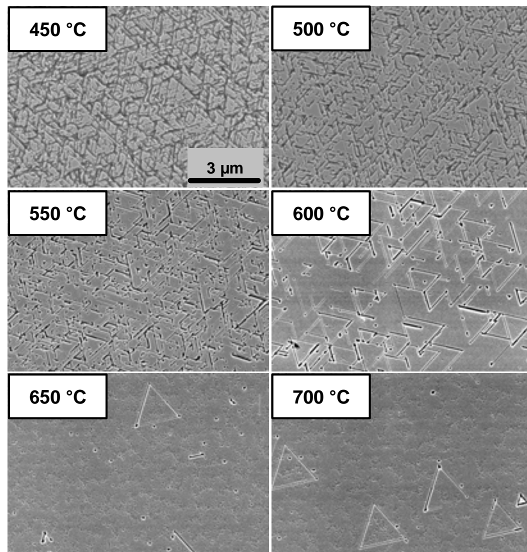

Figure 1: SEM images of Secco-etched Si films grown on Si(111) wafers at T_s= 450-700 °C with r_{si}= 60-75 nm/min. The Si films grown on (100) oriented Si wafers have shown no etch pits in this temperature range.

The strong influence of T_s on the etch pit density (triangles and holes) is clearly visible. The extended defect density decreases by increasing T_s. At $T_s \leq 550$ °C, a high density of extended defects has been created (above 10^8 cm^{-2}). For $T_s \geq 600$ °C, the etch pit density decreases dramatically down to 4×10^6. The etch pits in the form of triangles are typical for stacking faults in Si(111) epitaxy, whereas holes identify dislocations [14]. From the size of the triangles it is possible to calculate the origin depth of the stacking faults. From Figure 1 (T_s= 700 °C), for the big triangles having a length of about 2µm, a depth of about 1.7 µm can be calculated. This depth corresponds to the thickness of this film. Thus these defects were created at the epitaxial film / Si wafer interface. Analysing statistically the whole temperature range, it is found that many defects were generated at the epitaxial film / Si wafer interface. This can be related to the fact that we apply no in-situ cleaning of the substrate. The substrate surface conditioning is of great importance for a high quality epitaxy. Also triangles with smaller sizes can be seen in Figure 1. They correspond to the defects which were generated within the bulk of the epitaxial film. This can be attributed to the non-UHV conditions of our e-beam evaporation.

The influence of the deposition rate on the extended defect density is presented in Figure 2. The films investigated were grown on Si(111) wafers at T_s= 600 °C. The deposition rate has been varied from 40 to 475 nm/min. Thereby doping level of the films was held nearly constant. It is clearly seen that a higher density of extended defects were generated at higher r_{Si}. The lowest etch pit density of 1.7×10^7 cm^{-2} was obtained for r_{Si}= 40 nm/min. Whereas, the etch pit density is $\geq 10^8$ cm^{-2} for $r_{Si} \geq 185$ nm/min. This result of increasing extended defect density with increasing film growth rate is well known from Si epitaxy by Molecular Beam Epitaxy (MBE) [15].

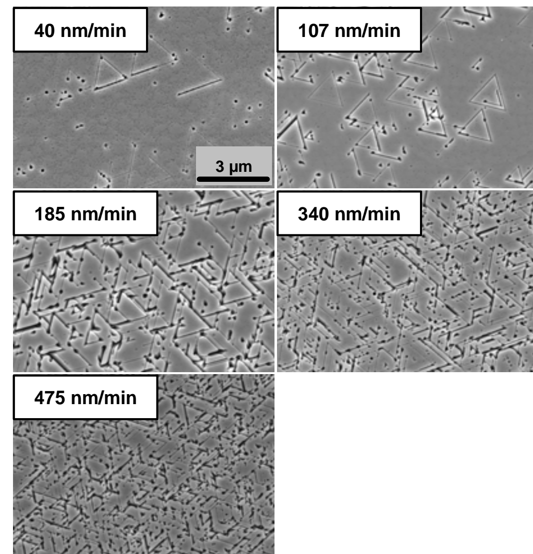

Figure 2: SEM images of Secco-etched Si films grown on Si(111) wafers at T_s= 600 °C with r_{Si}= 40-475 nm/min.

Extended defect etching experiments have been also performed on the films grown on poly-Si seed layers. An SEM image of a film grown at T_s= 600 °C after Schimmel etching is shown in Figure 3 (see experimental details). A grain with almost 10 µm size is visible. After defect etching, the grain exhibits only circular etch pits that are characteristic for dislocations. No triangles are visible. Comparing to our results on Si(100) wafers, we assume that this grain exhibits a (100) crystallographic orientation and the dislocations are mainly caused by the seed layer imperfections. From Figure 3, it is seen that this grain is surrounded by regions which are stronger etched. In order to analyse these regions, a more detailed study has been performed by using EBSD.

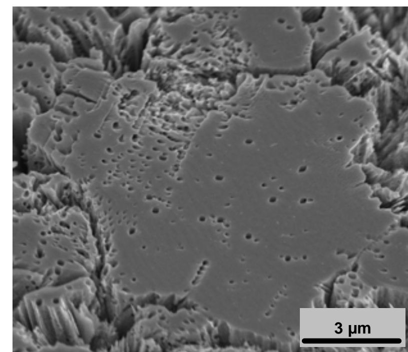

Figure 3: SEM image of a Schimmel-etched Si film grown on a poly-Si seed layer at T_s= 600 °C with r_{Si}= 150 nm/min.

Figure 4 presents a Secco-etched poly-Si film grown at T_s= 600 °C together with its corresponding EBSD color encoded orientation map. This figure shows the sample surface in a smaller magnification than Figure 3.

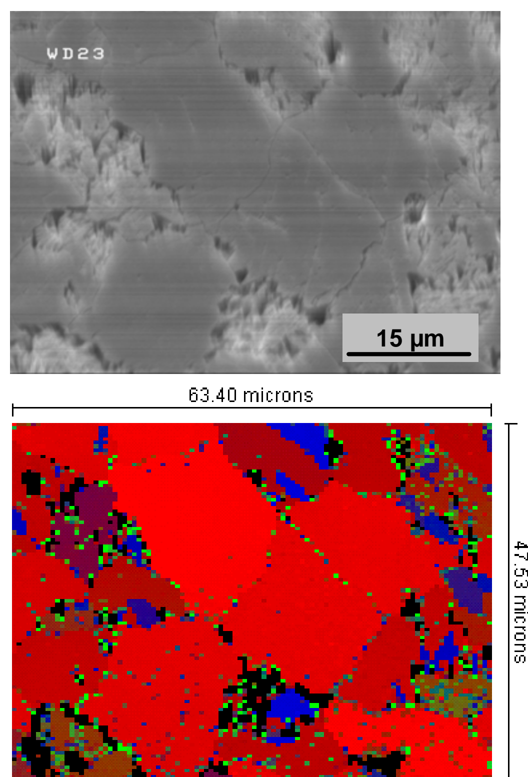

Figure 4: SEM image of a Secco-etched Si film grown on a poly-Si seed layer at T_s= 600 °C with r_{Si}= 150 nm/min and its corresponding EBSD color encoded orientation map. (Color coding: red (100), blue (111), green (110))

The large grains (in the center of Figure 4) exhibit an almost smooth surface even after defect etching. EBSD analysis shows that these grains have a (100) crystallographic orientation (red). The stronger etched grains exhibit mainly (111) (blue) or tilted of (100) (dark red) crystallographic orientations. Black regions correspond to parts which could not be analysed. This result agrees well with the results of defect etching experiments on epitaxial layers grown on Si(100) and Si(111) wafers. Almost no etch pits were observed on the smooth films grown Si(100), whereas about 10^8 cm^{-2} etch pits could be detected on films grown on Si(111) at T_s= 600 °C . As a summary, the grain orientation distribution of the underlying seed layer has a great influence on the epitaxial quality of the growing poly-Si film.

Analysing the SEM images (as well as optical light microscope images) of the films after defect etching, it was found that about 60% of the total sample surface exhibits less defective grains. This finding agrees well with the EBSD measurements of our seed layers which reveal 60% of the grains are preferentially (100) oriented [16]. As shown, this orientation is favourable for low defective epitaxial growth.

3.2 Electrical Properties

The temperature dependent Hall effect measurements of Si films grown on Si(100) and Si(111) wafers at T_s= 600°C with r_{Si}= 60 nm/min are presented in Figure 5. The two measured curves almost perfectly fit for the whole measurement range. An identical majority carrier scattering mechanism can be concluded. At room temperature the hole mobility is about 185 cm^2/Vs and the free carrier density amounts to about 8 x10^{16} cm^{-3}. From the Secco etching experiments, we obtained that epitaxial layers on Si(100) and Si(111) exhibit quite different density of extended defects. Obviously, the extended defects do not influence the Hall mobility.

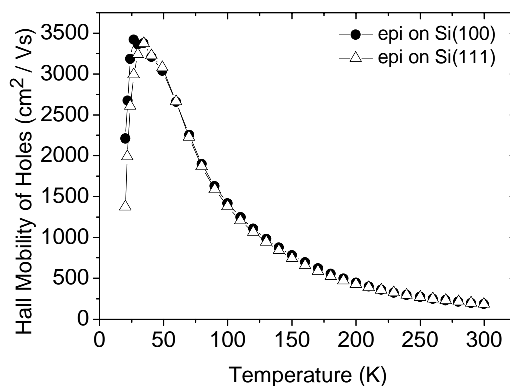

Figure 5: Temperature dependence of Hall mobility of holes measured on epitaxially grown Si films at T_s= 600 °C on Si(100) wafer (circle), and Si(111) wafer (triangle) with r_{Si}= 60 nm/min.

The influence of T_s and r_{si} on the hole mobility have been investigated on the films grown on Si(100) wafers. Figure 6 shows the room temperature hole mobility as a function of T_s in the range of 450-700 °C with r_{si}= 60-75 nm/min. The free carrier concentration is about 3-8 x10^{16} cm^{-3}.

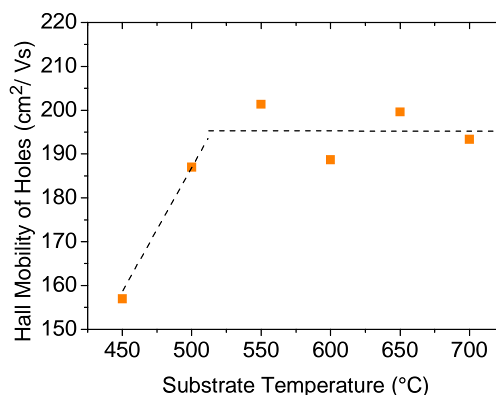

Figure 6: Room temperature Hall mobility of holes as a function of T_s in the range 450-700 °C with r_{si}= 60-75 nm/min measured on the films grown on Si(100) wafers.

For $T_s \leq$ 500 °C, the hole mobility decreases. The mobility is below 160 cm^2/Vs for T_s= 450 °C and about 185 cm^2/Vs for T_s= 500 °C. For $T_s \geq$ 550 °C, the mobility increases to about 195 cm^2/Vs and does not change further in the higher temperature regime. However, comparing our best experimental value of 200 cm^2/Vs to the mobility of 300 cm^2/Vs of perfect crystalline Si

within the dopand concentration range of the samples, this value is still too low [17]. We attribute this to carrier scattering by point defects which were not decorated by the defect etching procedures. From our experimental results it follows, that for $T_s \leq 500$ °C the mobility is dominated by an additional strong scattering mechanism.

In Figure 7, the hole mobility is presented as a function of r_{si} in the range of 40-475 nm/min for T_s= 600 °C. The free carrier concentration is about 3-9x10^{16} cm^{-3}. No significant influence of r_{si} on the hole mobility is obtained. Similar to the results of T_s variation, the mobility value is about 195 cm^2/ Vs.

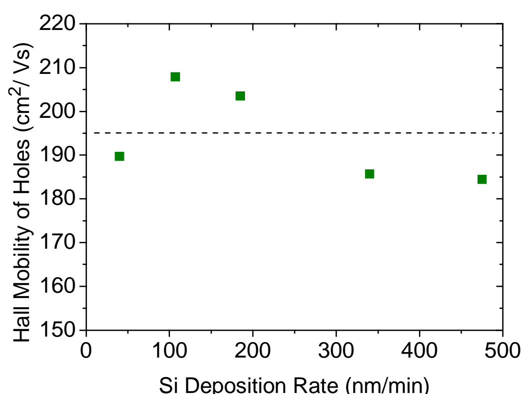

Figure 7: Room temperature Hall mobility of holes as a function of r_{Si} in the range of 40-475 nm/min at T_s= 600 °C measured on the films grown on Si(100) wafers.

3.3 Solar Cells

Figure 8 presents the current-voltage characteristics of the best wafer-based and the best glass-based solar cells of this investigation.

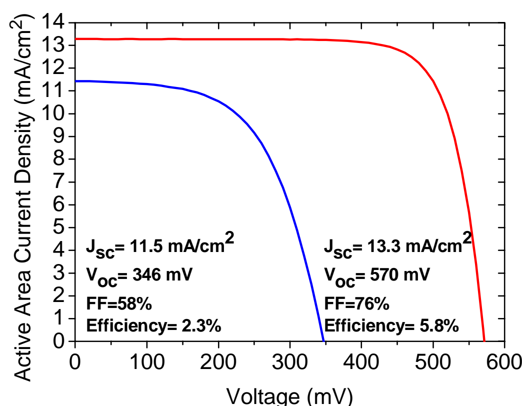

Figure 8: Active area current density versus voltage of solar cells (a) with an epi-Si film thickness of 1.8 µm on Si(100) wafer at T_s= 650 °C (red curve), (b) with an epi-Si film thickness of 2 µm on poly-Si seed layer on glass at T_s= 550 °C (blue curve).

The wafer-based solar cell has a 1.8 µm thick absorber layer deposited at T_s= 650 °C on Si(100), whereas the absorber layer of the glass-based cell was deposited at T_s= 550 °C with a thickness of 2 µm. Due to the glass substrate, no solar cells on glass could be prepared for the temperatures of 650 and 700 °C. The fact that the best cell is obtained at T_s= 550 °C instead of 600 °C needs to be further investigated to get better statistics.

The wafer-based solar cell is the best solar cell of this investigation. The efficiency of 5.8 % has been reached with an open circuit voltage of 570 mV, a short circuit current density of 13.3 mA/cm^2 and a fill factor of 76 %. The glass-based solar cell (measured with a white reflector) features an efficiency of 2.3%, an open circuit voltage of 346 mV, a short circuit current density of 11.5 mA/cm^2, and a fill factor of 58 %. However, comparing to the open circuit voltage of 570 mV for Si(100) wafer-based solar cell, the open circuit voltage of the glass-based solar cell is considerably low. The same concerns the fill factor. These results show that the poly-Si absorber layers still contain many defects, which are mainly caused by the seed layer imperfections.

4 CONCLUSIONS

Using electron beam evaporation, the effects of T_s and r_{Si} on the structural and electrical properties of the films grown on Si(111) and Si(100) wafers have been investigated. The films grown on Si(111) wafers exhibit a decreasing extended defect density as T_s increases and as r_{Si} decreases. The defect etching of the films grown on poly-Si seed layers reveals regions of quite different crystalline quality depending on the underlying crystallographic orientation. The temperature dependent Hall effect measurements of the films grown on Si(100) and Si(111) have shown that the extended defects do not significantly influence the hole mobility. However, the room temperature hole mobility is limited to about 195 cm^2/Vs. Further investigations will be performed to identify the origin of this carrier scattering mechanism. Open circuit voltages of 570 mV and 346 mV have been obtained for Si(100) wafer-based and glass-based solar cells, respectively. The results of the films on Si wafer substrates show that absorber layers can be grown by e-beam deposition at appropriate temperatures with solar grade quality. However, for glass-based solar cells, the seed layer properties together with the post-deposition treatments need to be improved to end up with reasonable solar cell parameters.

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6 REFERENCES

[1] S. Gall, J. Schneider, J. Klein, K. Hübener, M. Muske, B. Rau, E. Conrad, I. Sieber, K. Petter, K. Lips, M. Stöger-Pollach, P. Schattschneider, W. Fuhs, Thin Solid Films 511-512 (2006) 7-14.

[2] B. Rau, I. Sieber, J. Schneider, M. Muske, M. Stöger-Pollach, P. Schattschneider, S. Gall, W. Fuhs, Journal of Crystal Growth 270 (2004) 396-401.

[3] A. Straub, D. Inns, M. L. Terry, Y. Huang, P. I. Widenborg, A. G. Aberle, Journal of Crystal Growth 280 (2005) 385-400.
[4] G. Andrä, J. Bergmann, A. Bochmann, F. Falk, E. Ose, S. Dauwe, T. Kieliba, Proceedings of 20th European Photovoltaic Solar Energy Conference, Barcelona, Spain (2005) 1171-1174.
[5] C. W. Teplin, H. M. Branz, K. M. Jones, M. J. Romero, P. Stradins, S. Gall, Mater. Res. Soc. Symp. Proc. 989 (2007) A06-16.
[6] B. Gorka, P. Dogan, I. Sieber, F. Fenske, S. Gall, Thin Solid Films 515 (2007) 7643-7646.
[7] P. Dogan, B. Gorka, F. Fenske, I. Sieber, S. Gall, Proceedings of 21st European Photovoltaic Solar Energy Conference, Dresden, Germany (2006), p. 1060.
[8] S. Gall, K.Y. Lee, P. Dogan, B. Gorka, C. Becker, F. Fenske, B. Rau, E. Conrad, B. Rech, Proceedings of 22nd European Photovoltaic Solar Energy Conference, Milan, Italy (2007) (this conference).
[9] F. Secco d´Argona, J.Electrochem. Soc. 119 (1972) 948-951.
[10] D. G. Schimmel, J.Electrochem. Soc. 123 (1976) 734-741.
[11] M. Schmidt, H. Angermann , E. Conrad, L. Korte, A. Laades, K. v. Maydell, Ch. Schubert, R. Stangl, Proceedings of WCPEC 4, Waikoloa (2006), p. 1433-1438.
[12] B. Rau, K.Y. Lee, P. Dogan, F. Fenske, E. Conrad, S. Gall, Proceedings of 22nd European Photovoltaic Solar Energy Conference, Milan, Italy (2007) (this conference).
[13] B. Gorka, B. Rau, K.Y. Lee, P. Dogan, F. Fenske, E. Conrad, S.Gall, B. Rech, Proceedings of 22nd European Photovoltaic Solar Energy Conference, Milan, Italy (2007) (this conference).
[14] S. Mendelson, J. of Appl. Phys. 5 (1964) 35.
[15] Y. Ota, Thin Solid Films 106 (1983) 3-136.
[16] K.Y Lee, M. Muske, I. Gordon, M. Berginski, J. D'Haen, J. Hüpkes, S. Gall, B. Rech, EMRS 2007 Spring Conference (in press).
[17] D. A. Antoniadis, A. G. Gonzalez, R. W. Dutton, J.Electrochem. Soc. 813 (1978) 125.