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Breaking Barriers: Centimeter-Sized Single Layer WSe_2 by Gold-Mediated Exfoliation for Ambipolar Field Effect Transistors at Ultra-Low Voltages

Sarah Grützmacher, Wenkai Liu, Max Heyl, Patrick Amsalem, Norbert Koch, Emil J. W. List-Kratochvil, and Giovanni Ligorio**

Transition Metal Dichalcogenides (TMDCs) are promising semiconductor alternatives to silicon in CMOS technology. Their layered nature allows scaling to a single layer (1L) without degrading electrical performance, enabling further miniaturization of field-effect transistors (FETs). TMDCs like WSe_2 exhibit ambipolar transport, allowing fabrication of both *p*-type and *n*-type devices on a single flake, simplifying circuit design. Ambipolar, large-area, high-quality 1L-WSe_2 is therefore highly desirable. Here, centimeter-scale exfoliated 1L-WSe_2 is achieved, reaching 1L areas of up to 20 mm^2 via thermally activated gold-mediated TMDC exfoliation using large, high-quality WSe_2 parent crystals. The quality of 1L-WSe2 is comprehensively investigated via Raman spectroscopy, photoluminescence, X-ray, and ultraviolet photoelectron spectroscopy, as well as electronic transport measurements. For the latter, 1L-WSe_2-based FETs are fabricated on lithium-ion conducting glass ceramic substrates serving as both supporting substrate and high-performance gate. Subthreshold slopes as steep as 30 and 50 mV dec^{-1}, maximum mobilities of 15 and 18 $cm^2\ V^{-1}\ s^{-1}$, and ON/OFF ratios of ≈10^8 and 10^9 for electron and hole currents, respectively, are achieved at ultra-low gate voltages (≈2 V). The performance, demonstrated across 15 devices, suggests that 1L-WSe_2 in this device architecture can pave the way toward providing an alternative to conventional silicon-based CMOS technology for innovative, further miniaturized devices.

1. Introduction

Conventional silicon-based complementary metal-oxide-semiconductor (CMOS) technology is reaching its scalability limit in the miniaturization of field-effect transistors (FETs).[1–5] To maintain effective electrostatic control of the channel by the gate electrode, a body thickness of less than one-third of the gate length is the general guideline.[6,7] However, the downscaling of 3D bulk semiconductors, such as silicon, is compromised by surface roughness, the reaction of dangling bonds upon interface formation, and thickness fluctuations, which induce charge carrier scattering and ultimately result in poor device performance.[2,4,8,9]

In this regard, 2D transition metal dichalcogenides (TMDCs) have long caught the attention of the semiconductor industry.[1,2,4,5,10,11] TMDCs (MX_2, where M = group IV–VII metal and X = chalcogen) are layered crystalline materials where the three-atom-thick layers are held together by weak van der Waals (vdW) forces. This allows for downscaling to single-layer (1L) thickness while maintaining excellent charge carrier transport properties due to the atomically sharp, dangling-bond-free structure of the individual 2D sheets.[2,12–16] Within the TMDC family, tungsten diselenide (WSe_2) displays excellent properties in devices, such as high charge carrier mobility (up to 150 $cm^2\ V^{-1}\ s^{-1}$),[17] near-ideal subthreshold swing in FETs (SS ≈ 60 mV dec^{-1}), and large ON/OFF current

S. Grützmacher, W. Liu, M. Heyl, P. Amsalem, N. Koch, E. J. W. List-Kratochvil, G. Ligorio
Institut für Physik
Humboldt-Universität zu Berlin
Zum Großen Windkanal 2, 12489 Berlin, Germany
E-mail: emil.list-kratochvil@hu-berlin.de; giovanni.ligorio@hu-berlin.de

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S. Grützmacher, W. Liu, M. Heyl, E. J. W. List-Kratochvil, G. Ligorio
Institut für Chemie
Humboldt-Universität zu Berlin
Zum Großen Windkanal 2, 12489 Berlin, Germany

S. Grützmacher, W. Liu, M. Heyl, P. Amsalem, N. Koch, E. J. W. List-Kratochvil, G. Ligorio
Center for the Science of Materials Berlin
Zum Großen Windkanal 2, 12489 Berlin, Germany

N. Koch, E. J. W. List-Kratochvil
Helmholtz-Zentrum Berlin für Materialien und Energie GmbH
Hahn-Meitner-Platz 1
14109 Berlin, Germany

ratios (>10^6).[6,11,17,18] Furthermore, unlike MoS_2, which predominantly shows unipolar n-type behavior, WSe_2 displays ambipolarity, which refers to the ability to conduct both electrons and holes.[13,17,19,16]

The use of ambipolar materials, which can be seamlessly switched between p-type and n-type conduction by applying an electric field, opens up new possibilities for CMOS or CMOS-like technologies.[7,14] While in silicon CMOS technology the type of conductivity is controlled via substitutional doping,[20,21] doping in 2D TMDCs is achieved via chemical or contact doping.[6,19,22–25] Moreover, there has been growing interest in exploring doping-free alternatives.[7,12,14,20,21,26,27] This includes, for example, the engineering of contacts to enhance either electron or hole transport,[6,23,26,28] or the circuit engineering such that the same ambipolar transistors can be used to construct CMOS-like circuits.[12,20,21,27,29,30] Henceforth, to further drive this promising avenue of innovative, beyond-CMOS technology, the reliable fabrication of high-quality, large-area ambipolar materials, such as 1L-WSe_2, is in ever-growing demand.

Despite intensive research into bottom-up methods, such as chemical vapor deposition (CVD) and molecular beam epitaxy, the top-down method mechanical exfoliation, remains the most accessible technique for reliably producing high-quality 1L TMDCs.[31–35] CVD can consistently produce uniform films over large areas, which is crucial for future commercial applications. However, 1Ls produced with this technique often do not deliver high quality 1Ls. Mechanical exfoliation, on the other hand, delivers 1L-TMDCs with very few defects and excellent crystallinity where a high-quality parent crystal is available, which is essential for fundamental research and for applications requiring high-performance electronic and optical properties. Additionally, the exfoliation process is straightforward and does not require expensive equipment, which makes it more accessible for laboratory research.

The historical (top-down) Scotch tape method was first discovered for exfoliating 1L-graphene almost 2 decades ago.[36] While this method, applied to TMDCs, delivers high quality 1L, the scalability is limited to less than 100 µm.[33,37] To address this challenge, Magda et al. introduced a gold-mediated exfoliation technique in 2015, which enabled the exfoliation of 1L-MoS_2 with dimensions of several hundreds of microns.[38] The strong affinity between gold (Au) and chalcogens results in enhanced adhesion between TMDC and Au compared to TMDC interlayer adhesion, thereby increasing the probability of cleaving the topmost layer.[32,39–42] Since then, the Au-mediated technique has been optimized, enabling the production of 1L-MoS_2 with areas up to 82 mm^2.[35] While direct evaporation of Au onto the TMDC crystal induces defects in the TMDC,[33,43] high-quality 1L-TMDC can be obtained employing the template-strip method.[33,35,44,45] This method involves cleaving an Au (or other metal) film from an ultra-smooth template substrate, such as a polished SiO_x wafer, to produce equally smooth, pristine Au surfaces. The freshly cleaved, uncontaminated and smooth Au surface facilitates ideal Au/TMDC vdW interaction – essential for overcoming TMDC interlayer interactions – enabling the exfoliation of the topmost layer.[32] Although the Au-mediated exfoliation process can be applied to a wide range of TMDCs,[41] the focus so far has mainly been on producing millimetre-sized 1Ls of n-type 1L-MoS_2. However, there is an urgent need for similarly sized 1Ls of ambipolar TMDCs, such as WSe_2.

In this work, we report the exfoliation of centimeter-sized 1L-WSe_2. This is achieved by combining the template strip method for the Au-mediated exfoliation with the use of high-quality, large area WSe_2 crystals. 1L-WSe_2 of up to 20 mm^2 is achieved with little to no multilayer (nL) regions. We observed that the 1L size is solely limited by the parent crystal employed. Utilizing a polymer-free, Au-assisted transfer we deposit the 1L-WSe_2 without observable loss in size or quality on relevant target substrates. The quality of the 1L before and after the transfer is investigated via Raman, photoluminescence (PL), as well as X-ray and ultraviolet photoelectron spectroscopy (XPS and UPS). The ambipolar transport behavior of the 1L-WSe_2 is demonstrated by the fabrication of FETs, using lithium ion conducting glass ceramic (LiCGC) as gate. LiCGC is a solid electrolyte, which serves both as the supporting substrate and as the gate and allows the operation of the FETs at ultra-low voltages. From the output and transfer curves the key device characteristics, such as subthreshold swing, ON/OFF ratios, mobility and threshold voltages, are extracted with high reproducibility.

2. Results and Discussion

2.1. Fabrication of Exfoliation Substrate

The metal-mediated exfoliation method relies on the adhesion between metals, such as Au and Ag (silver), and the outer layer of the TMDC crystal.[32,35,44,46] Achieving conformal, uncontaminated contact (undisrupted by surface contamination) between the two is essential for ideal vdW interactions.[32,41] To accomplish this, the template-strip method was employed to create a pristine, ultra-smooth metal surface on the exfoliation substrate. We previously reported this technique for the exfoliation of centimeter-sized single layer (1L) MoS_2, where the 1L area is solely limited by the size of the parent crystal.[35]

The illustration in **Figure 1a** depicts the fabrication steps for the exfoliation substrate via the template-strip method. A highly polished Si wafer with native oxide was selected as the template due to its ultra-low surface roughness (root mean square (RMS) ≈0.3 nm).[47,48] The wafer was cleaned via sonication and treated with oxygen plasma to remove organic residue (see experimental section for detailed procedures). Subsequently, a thin film of Au (≈100 nm) was deposited via physical vapor deposition, followed by the deposition of a Cu layer (≈900 nm)—see i) in Figure 1a. Glass slides (1 × 1.5 × 0.5 mm) were then affixed onto the Au/Cu template using epoxy resin. Upon curing the epoxy resin with UV light (90 min), the glass slide with the metal stacks glued to it is peeled off the silicon wafer (template strip)—see ii) and iii) in Figure 1a. This yields a batch of ultra-smooth (RMS ≈ 0.3 nm) exfoliation substrates (see Figure S1 in the Supporting Information).

2.2. Exfoliation

The exfoliation substrates (Au/Cu/epoxy/glass) are employed for the exfoliation of WSe_2. To reduce contamination of the Au surface and ensure conformal contact between Au and WSe_2, it is

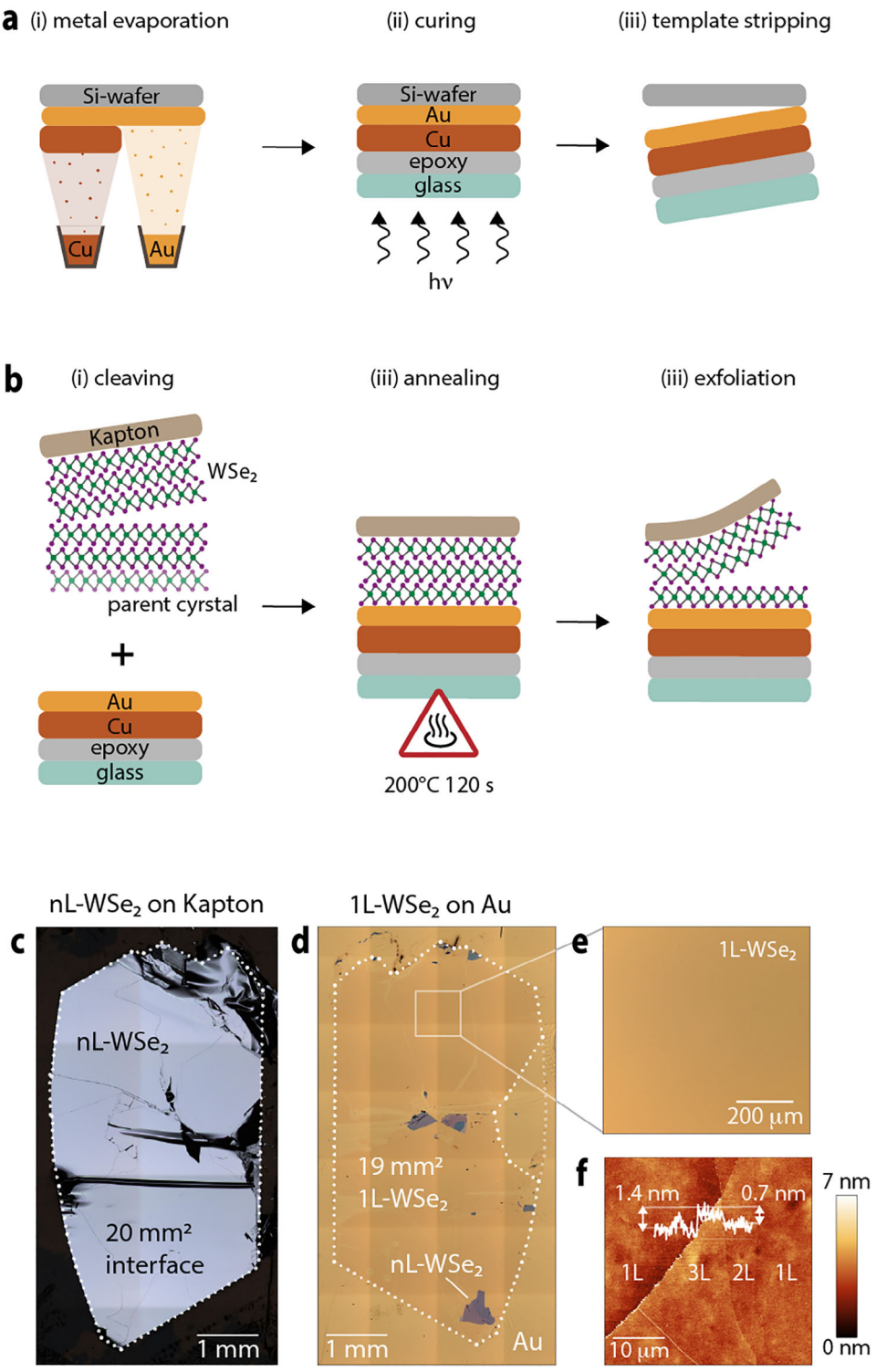

Figure 1. a, b) Schematic illustration of the exfoliation substrate preparation and the exfoliation procedure, respectively. c, d) Optical microscope images of nL-WSe_2 on Kapton tape and the corresponding exfoliated 1L-WSe_2 on Au, respectively. The TMDC is outlined and measures 20 and 19 mm^2, respectively. e) Zoom-in of the 1L-WSe_2 area from image (d). f) SFM image of 1L, 2L, and 3L WSe_2, displaying a step height of 0.7 nm from layer to layer.[2,3]

important to use the exfoliation substrate directly after the template stripping. The procedural steps are schematically illustrated in Figure 1b. Thermally stable Kapton tape is used to cleave few-layer WSe_2 from the parent crystal – see b i). Figure 1c displays an optical microscope image of the multilayer (nL) WSe_2 on the tape. The effective area of the parent crystal on Kapton measures 20 mm^2, excluding wrinkled areas that do not make contact with the exfoliation substrate. After achieving a pristine, uncontaminated WSe_2 surface on the Kapton tape, it is brought into contact with the exfoliation substrate – see ii) in Figure 1b. Heat treatment at 200 °C for 2 min is employed to enhance the adhesion between the exfoliation substrate and WSe_2. This temperature and time were established as ideal for achieving the largest 1L exfoliation in our previous work and proved to be the most effective in this study as well. The Kapton tape is then peeled off the substrate, leaving 1L-WSe_2 on the Au surface of the exfoliation substrate – see iii) in Figure 1b.

Figure 1d displays an optical microscope image of the exfoliated 1L-WSe_2 on the Au substrate, which is the mirrored image of the nL-WSe_2 on the Kapton tape (Figure 1c). The white dotted line serves as a guide to identify the TMDC. Based on previous work,[35,44] the large, slightly darker-than-gold regions (outlined) were identified as monolayers, while the colored regions correspond to multilayers. The monolayer's continuity over several square millimeters can be clearly seen, covering an area of 19 mm^2 – corresponding to a 1L yield of 96% relative to the parent crystal. Small areas with distinct color contrast, attributed to multilayers and confirmed by SFM analysis (see below), account for ≈1% of the total area. Figure 1e provides a zoom-in of a 1L region from Figure 1d, illustrating its homogeneity.

It is worth mentioning that pristine WSe_2 can be obtained, as mentioned above, by cleaving the parent crystal with Kapton tape as well as by cleaving the used tape (which has nL-WSe_2 on it) with a fresh tape. However, as expected, with each cleaving of the used tape, the crystal becomes increasingly wrinkled, and the 1L yield decreases while the nL yield increases. This is due to limitations in contact between the TMDC crystal and Au caused by the wrinkled areas, resulting in a decreased effective area of the parent crystal (see Figure S3, Supporting Information). However, we find the average yield (when exfoliating with a new tape and cleaving from the parent crystal) to be reliable ≈97% 1L area with respect to the effective parent crystal area (see Figure S4, Supporting Information).

Scanning force microscopy (SFM) was employed to investigate the 1L quality on the nanometer scale. A spot with a multilayer region was chosen to measure the step height from layer to layer. The obtained lateral profile is shown in Figure 1f, displaying the height cross-section measured moving from one layer (1L) to two layers (2L) to three layers (3L). The relative step height between the layers is 0.7 nm, as reported in the literature.[49,50] See Figure S2 (Supporting Information) for the respective optical microscopy image.

2.3. Transfer of 1L-WSe_2

For applications, it is essential to devise a suitable strategy for transferring the single layer onto the desired surface or device. Following this consideration, the previously reported polymer-free gold-mediated transfer procedure was employed after exfoliating large area 1L-WSe_2.[35]

The illustrations in **Figure 2a** schematically depicts the steps for transferring 1L-WSe_2 from the exfoliation substrate to the desired target substrate. The exfoliation substrate i) with 1L-WSe_2 is placed in an aqueous $FeCl_3$ (33 wt.%) solution ii) to etch the Cu layer and thereby separate the Au/WSe_2 layer from the glass/epoxy layer. Once the Cu layer is fully etched away, the Au/WSe_2 foil floats freely on the $FeCl_3$ solution. A clean glass slide is employed to "fish" out and transfer the foil into a beaker with deionized water iii). To fully remove $FeCl_3$ residues, this process is repeated twice (or until the water is clear). To overcome the high surface tension of water and to fully immerse the foil in the solvent, the Au/WSe_2 foil (with WSe_2 facing upward) is transferred into isopropyl alcohol (IPA). This allows the film to sink and carefully be flipped using tweezers. The WSe_2/Au foil (with WSe_2 now facing downward) can then be transferred onto the target substrate v). The transfer can be achieved by "fishing" the foil from the solution with the target substrate. Another option is to carefully place the target substrate in the IPA beneath the sunk foil and remove the IPA with a pipette or syringe. Subsequently, the Au foil is gently pressed onto the target substrate by carefully blowing it with N_2, which minimizes solvent residue on the substrate. The sample is left to dry at room temperature for 1 h. Two heat treatment steps are then employed. The first step (80 °C, 30 min) gently removes any remaining solvent between the target substrate and the Au foil. The second step (150 °C, 30 min) ensures conformal contact between WSe_2 and the substrate for ideal vdW interaction, ensuring that the 1L stays on the substrate when the Au is etched away. The Au etching vi) is achieved by applying KI/I_2 etchant (Sigma Aldrich, "Au etchant, standard") to the Au foil with a pipette. After 30 min, the sample is rinsed with acetone and IPA, leaving centimeter-sized 1L-WSe_2 on the target substrate vii).

2.4. Characterization of 1L-WSe_2

Figure 2b shows the optical microscope image of the 1L-WSe_2 (displayed in Figure 1d on Au) after transfer to the target substrate (in this case, a lithium ion conducting glass ceramic, LiCGC; see below for further details regarding this substrate). For better contrast, a polarized detection scheme was used for the microscope images.[51] The 1L area, visible in the light brown contrast, is 18.8 mm^2, corresponding to 99% of the 1L area on Au before the transfer (see Figure 1d). For this specific sample, the nL area, visible in the black contrast, is only 3% of the total WSe_2 area.

The quality of the transferred 1L was assessed as follows. The Raman spectrum of 1L-WSe_2 on the LiCGC substrate is shown in Figure 2c. The spectrum displays the typical in-plane vibration $E^1{}_{2g}$ and the out-of-plane vibration A_{1g}, centered at 248.5 and 260.7 cm^{-1}, respectively.[52,49] The photoluminescence (PL) spectrum, shown in Figure 2d, is characterized by a strong emission peak centered at 1.65 eV, confirming the excellent 1L quality.[52,49]

Chemical analysis with X-ray photoelectron spectroscopy (XPS) was performed for WSe_2 on the Au exfoliation substrate, as well as on two other relevant target substrates: SiO_x (Si with a native oxide layer) and LiCGC. WSe_2 was transferred following the above-described transfer process. The corresponding W(4f)

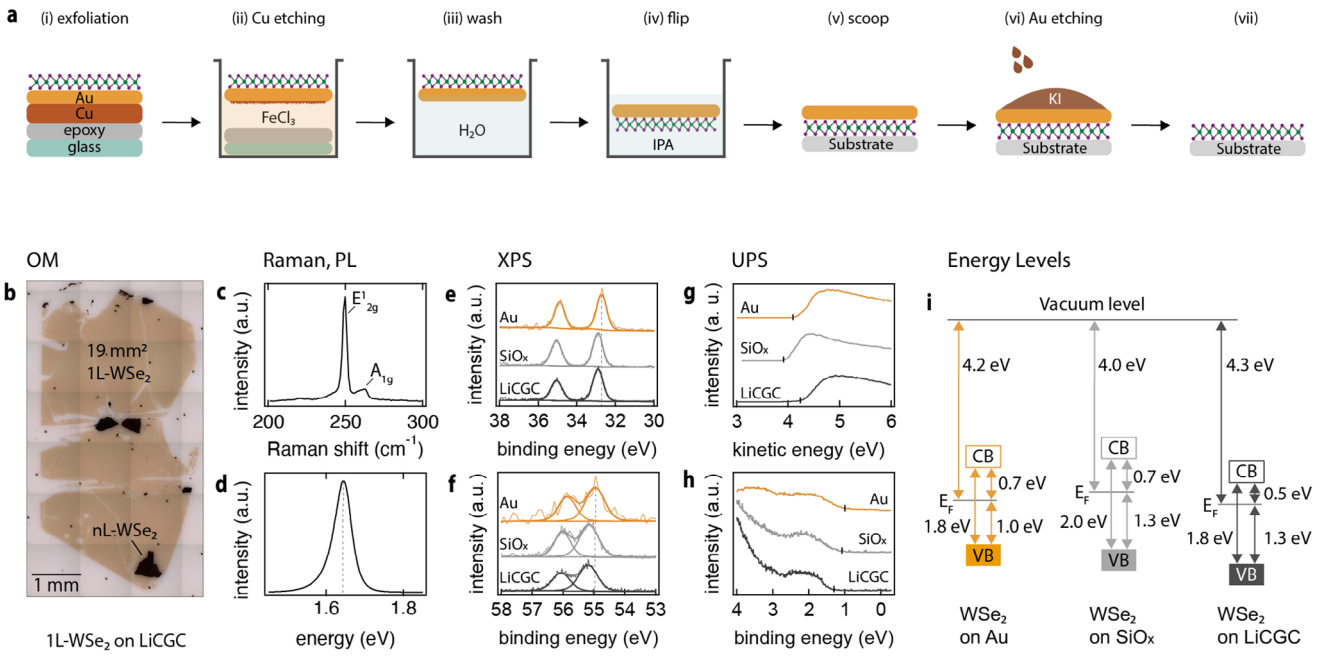

Figure 2. a) Schematic illustration of the metal-assisted transfer of exfoliated 1L-WSe_2. b) Optical microscope image of transferred 1L-WSe_2 on a LiCGC substrate. c) Raman spectra of WSe_2, displaying the for 1L typical in-plane vibration E^1_{2g} and the out-of plane vibration A_{1g} frequency centered at 248.5 and 260.7 cm^{-1}, respectively.[1,2] d) PL spectra of 1L-WSe_2 with emission at 1.65 eV.[1,2] e, f) XPS spectra of W(4f) and Se(3d) core levels, respectively, on Au, SiO_x and LiCGC substrate. The W($4f_{7/2}$) and W($4f_{5/2}$) doublet is centered at 33 and 35 eV. The Se(3d) core level show the doublet of Se($3d_{5/2}$) and Se($3d_{3/2}$) core levels at 55 and 56 eV. g, h) Secondary electron cut off (SECO) and valence band (VB) spectra of WSe_2 on Au, SiO_x and LiCGC substrate. i) Schematic illustration of the energy levels of WSe_2 on Au, SiO_x, and LiCGC, respectively.

and Se(3d) core levels are shown in Figure 2e,f. The W(4f) core level doublet shows two peaks at 34 and 35 eV, corresponding to $4f_{7/2}$ and $4f_{5/2}$ of W^{4+} from WSe_2, respectively. These values are in agreement with previous reports.[52,25] The doublet is shifted toward higher binding energy by 0.2 eV on the SiO_x and LiCGC substrates compared to the position of the core level measured on the Au substrate used for exfoliation. An overview of the core level peak positions on the different substrates can be found in Table S1. The spectrum of the Se(3d) core level shows the doublet at 55 and 56 eV, attributed to $3d_{5/2}$ and $3d_{3/2}$ of Se^{2-}, respectively.[25,53] The same shift to higher binding energies of 0.2 eV is observed on SiO_x and LiCGC substrates compared to the Au substrate (see below for more details). To demonstrate the complete removal of Au by the etchtant, the Au(4f) core level energy range is displayed for all three substrates. The 4f doublet, visible at 84.6 and 88.5 eV for the Au substrate, is absent in case of SiO_x and LiCGC substrate (see Figure S5, Supporting Information).

To gain information about the electronic properties of WSe_2 on the three substrates, the secondary electron cutoff (SECO) and valence band (VB) regions were investigated by ultraviolet photoelectron spectroscopy (UPS). Figure 2g,h display the SECO and VB spectra, respectively, from which the work function (Φ) and the hole injection barrier (HIB) were extracted. The Φ, determined as the difference between the vacuum level and the Fermi level (E_F), is smaller on SiO_x (3.95 eV) compared to the values measured on Au and LiCGC (4.20 and 4.30 eV, respectively). The HIB, determined as the difference between the VB onset and E_F, is larger on SiO_x and LiCGC (0.24 and 0.31 eV, respectively) compared to the value measured on Au (1.01 eV). The HIB can be used to predict the n-/p-nature of a semiconductor if the value of E_g is known. However, it is crucial to accurately estimate the value of E_g for 2D TMDCs. Unlike conventional bulk semiconductors, E_g is not a constant value for this class of materials due to its high sensitivity to its dielectric environment. As demonstrated in our previous reports,[54,55] the E_g of 2D TMDCs is highly dependent on dielectric screening by the supporting substrate. An accurate value for E_g can be calculated via the expanded Schottky-Mott rule as:

$$E_g\left(\varepsilon_r\right) = E_g\left(\varepsilon_r = \infty\right) + \alpha/\varepsilon_r \quad (1)$$

where $E_g(\varepsilon_r)$ is the band gap of the TMDC on a substrate with the dielectric constant ε_r, $E_g(\varepsilon_r = \infty)$ is the band gap of the TMDC on a substrate with infinite dielectric constant ($\varepsilon_r = \infty$) and α is an empirical constant. For detailed explanation, we refer the reader to our previous reports.[54,55] **Table 1** summarizes the energy

Table 1. Energy level of WSe_2 on Au, SiO_x and LiCGC. The value for $E_g(\varepsilon_r = \infty)$ is taken from literature.[56] $E_g(\varepsilon_r)$ was calculated according to Formula 1. All values are given in eV.

	Φ	HIB	E_g [$\varepsilon_r = \infty$]	E_g [ε_r]	EIB
WSe_2 on Au	4.20	1.01	1.75	1.75	0.74
WSe_2 on SiO_x	3.95	1.25	1.75	1.98	0.73
WSe2 on LiCGC	4.30	1.32	1.75	1.78	0.46

levels for WSe_2 on the three different substrates. The reported values for Φ and HIB are experimentally measured via UPS. The $E_g(\varepsilon_r)$ is calculated employing the expanded Schottky-Mott rule as given above. The electron injection barrier (EIB) is calculated as the difference between $E_g(\varepsilon_r)$ and the HIB. The value for $E_g(\varepsilon_r = \infty)$ is taken from our previous report[56] for WSe_2 on Au (1.75 eV), considering ε_r for metal infinite. The value for ε_r for LiCGC and SiO_x were taken from literature and are 35 and 3.9, respectively.[57,58] An empirical value α of 0.9 eV was chosen according to previous reports.[54,55] Figure 2i shows a schematic illustration of the energy level of WSe_2 on the three substrates. WSe_2 on Au exhibits a E_g of 1.8 eV with a HIB of 1.0 eV and an EIB 0.7 eV. On the SiO_x and LiCGC E_g are calculated accordingly to Equation (1) to be 2.0 and 1.8 eV, respectively. Given the smallest dielectric constant of SiO_x in this series, the consequent renormalization of E_g on this substrate results in the largest. The measured HIBs are 1.3 eV (on both substrates) and the calculated EIB on SiO_x results the same as on Au (0.7 eV) and 0.5 eV on LiCGC. The results indicate that WSe_2 has n-character on all three substrates. However, on the SiO_x and LiCGC substrate the n-type character is stronger with respect to the Au substrate. This is consistent with the XPS measurements, where the Se(3d) and the W(4f) core levels exhibit a corresponding rigid shift toward higher binding energies, as a shift of the E_F should correlate with a shift of the core level binding energies.[25]

It should be mentioned that the VB spectra were measured at the γ-point with ± 10° integration angle. We notice that the obtained spectra are considerably broadened compared to literature, where a sharp and intense peak is usually reported at γ. This is attributed the sample surface not being atomically clean, as the sample did not undergo an additional in-situ cleaning procedure. As a result, incoherent scattering by surface contaminants occurs upon photoemission and no angular dispersion can be observed. This is because the spectra then represent an integration over the whole Brillouin Zone. Consequently, the determined VB onset of emission is attributed to the global VB maximum originating from the K-point.

2.5. Electric Characterization of Transferred 1L-WSe_2 in a FET

After the thorough characterization via various spectroscopic methods, the electronic properties of the of the 1L-WSe_2 are investigated in a FET. **Figure 3a** illustrates a schematic of the device cross section. Moving from bottom to top, the device consists of six layers: an Au/Cr layer, a LiCGC substrate and WSe_2 stacked with extension contacts consisting of a layer of Al_2O_3/SiO_x and Cr/Au, and a source and drain electrode consisting of Pt/Ag. The bottom Au/Cr layer serves as the gate contact. LiCGC was chosen for the fabrication of FET operating at ultra-low voltages. LiCGC is a solid-state electrolyte which is both the supporting substrate and a highly efficient gating material.[51,59] Its ability to work as a gating substrate in FETs originates from the formation of an electric double layer (EDL) when a bias is applied. The EDL has an extension of less than one nanometre at the interface with the channel material.[51] This results in a large effective capacitance (≈0.9 μF cm^{-2}, see Figure S6 for more details), allowing for high device performance at low-voltages.[51,59] The next layer of the device is 1L-WSe_2 which serves as channel material. When employing LiCGC substrates, the source and drain contacts (S and D) must be fabricated as small as possible. This minimizes undesired gate currents, originating from electrochemical reactions between Li^+ ions and the metal contacts.[51] Given the small dimension of the source and drain electrodes, it is necessary to fabricate extension contacts (ECs) used to externally connect the device. The extension contacts are electrically decoupled from the LiCGC substrate and WSe_2 by an insulating Al_2O_3/SiO_x layer. Al_2O_3 serves here as adhesion layer between LiCGC/WSe_2 and SiO_x.[51] The fabrication of the devices is discussed in detail in the experimental section. A microscope image of the channel region of a typical device is depicted in Figure 3b. The large golden contacts are the electrically decoupled ECs (Al_2O_3/SiO_x/Cr/Au), connected to the 20 × 50 μm 1L-WSe_2 channel via small-area Pt/Ag electrodes.

15 FETs were electrically characterized. The output and transfer curves were investigated and the ON/OFF ratio, the subthreshold swing (SS), the mobility (μ) and the threshold voltage (V_{th}) for electrons and holes were extracted from the curves. The devices displayed high reproducibly, which can be seen in a summary of the key characteristics in Figure S7 in the Supporting information. In the following text, we will discuss in detail the curves of one of the 15 devices. All measurements were performed in inert nitrogen atmosphere at room temperature.

A Typical output and transfer curve is reported in Figure 3c,d, respectively. The output curve in Figure 3c displays the source-drain current I_{ds} plotted against the source-drain voltage V_{ds} measured at different constant gate voltages V_g. The curve shows textbook-like transistor behavior, displaying a steep SS (200 mV/dec) in the linear region followed by an ideal saturation region identifying parabolic locus of pinch off voltage (indicated with the black dashed line). This ideal behavior reflects the high quality of the 1L-WSe_2 employed as channel material. The operation at low gate voltages is a consequence of the large effective capacitance achieved due to the EDL in the LiCGC substate.

The transfer measurements were conducted utilizing the dual channel pulsed I-V (PIV) method.[60] This approach involves a short turn-on time ($t_{on} = 10^{-2}$ s) followed by a long turn-off time ($t_{off} = 10^{-1}$ s) after each point of measurement. During t_{off} a base voltage ($V_{base} = V_g$ and V_{ds}) of 0 V is applied. This enables charge carriers to be released of bias stress caused by V_g and V_{ds} during t_{on} and effectively eliminates hysteric behaviors in TMDC FETs.[60]

The transfer curve displayed in Figure 3d in semi-logarithmic scale is the module of the source-drain current $|I_{ds}|$ plotted against the V_g measured at V_{ds} = 1 V (during t_{on}). The blue and red regions indicate where the electron and hole transport occur, respectively. The module of the gate current $|I_{gs}|$ is reported in the grey line. The arrows indicate the sweep direction. The device displays ambipolar transport behavior with SS of 100 and 140 mV dec^{-1} for electron and hole current, respectively. The ON/OFF current ratio is as high as six orders of magnitude, while the gate current remains below 2 nA. An upward and downward peak at −0.8 and 0.6 V, respectively, can be seen in the gate current. The peaks are attributed to hole and electron accumulation at the interface between LiCGC and the channel and we exclude electrochemical phenomena.[51] This interpretation is based on the measurement with a reference electrode. The reference

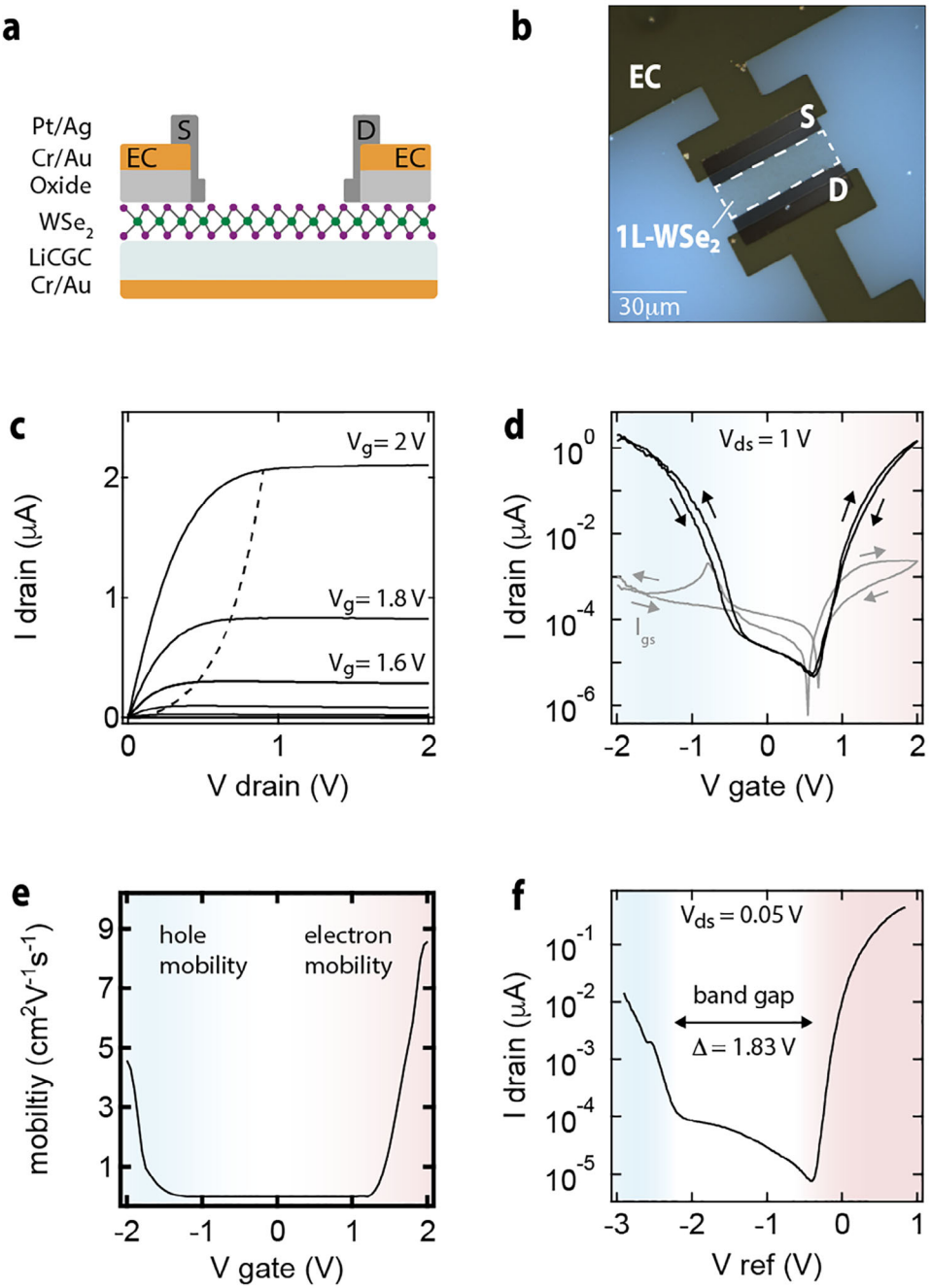

Figure 3. a) Schematic of the cross section of 1L-WSe_2 FETs on LiCGC substrates. b) Microscope image of a typical device comprised of extension, source, and drain contacts (S, D, ECs, respectively) with 1L-WSe_2 channel dimensions of 20 × 50 µm. c) Output characteristics LiCGC-gated 1L-WSe_2 FETs. d) Respective ambipolar transfer characteristics measured at V_{ds} = 1V. The red and blue regions indicate the electron and hole currents, respectively. The gate current I_{gs} is plotted in the same scale in grey, and the arrows indicate the sweep direction. e) Carrier mobility μ against V_g. f) The transfer curve measured at 0.05 V against V_{ref}, the potential measured with a reference electrode near the channel. The E_g can be extracted as $E_g = e(V^e_{th} - V^h_{th})$, with V^e_{th} and V^h_{th} representing the threshold voltages for the electron and hole currents. The E_g is 1.83 V.

electrode situated at near distance to the channel measures the potential V_{ref}. A linear dependence of V_{ref} to V_g indicates the absence of interfacial electrochemical reactions.[51] For more details see Figure S11 in the Supporting information.

It is worth mentioning that measuring the FETs with a conventional, continuous sweep allows to reach SS as steep as 30 and 50 mV dec^{-1}, ON/OFF ratios of up to 8 and 9 orders of magnitude for electron and hole currents, respectively (see Figure S11 in the Supporting information). These values set a new precedence for

LiCGC-gated 1L-WSe_2 FETs, with the SS being half the values as previously reported in literature.[51] However, these measurements suffer from hysteresis depending on the direction of the sweep, which we attribute to charge accumulations of Li^+ ions at the LiCGC-channel interface.

The low SS values of the devices indicate high quality of the channel and interface. From the SS the interface trap density D_{it} can be calculated.[12,61–64] The D_{it} is a key parameter for semiconductors, as it influences the SS and thereby the switching behavior of transistors. 2D material-based FETs often suffer from high D_{it}, which results in large SS and, due to limited electrostatic control, more power consumption.[64] The SS and the D_{it} relate via $SS = \frac{kT}{q} \ln(10) \left(1 + \frac{qD_{it}}{C_{ox}}\right)$, where k is Boltzmann constant, T the temperature, q the elementary charge and C_{ox} the capacitance per unit area of the gate (in this case the capacitance of the EDL of the LiCGC gate; for details see Figure S6 in the Supporting information). Values of $\approx 10^{13}$ $eV^{-1}cm^{-2}$ are obtained for the D_{it}, which is in good agreement with literature values for 1L-TMDC based FETs.[12,63,64]

The carrier mobility (μ) was extracted from the transfer measurements. Curves measured at 0.05 V were chosen and μ was obtained using the equation: $\mu = [L/(W \cdot C_{ox} \cdot V_{ds})] \cdot [dI_{ds}/dV_g]$, where L and W are the channel length and width and $[dI_{ds}/dV_g]$ the derivation of the curve I_{ds} against V_g. The mobility plotted against V_g is displayed in Figure 3e. Maximum electron and hole mobilities of 16 and 18 $cm^2V^{-1}S^{-1}$ are obtained (see Figure S12 in the Supporting information). Up to date there are no literature values for the mobilities for 1L-WSe_2 FETs from transfer curves of similar device structures. However, slightly higher values were measured employing Hall measurements on 1L-WSe_2 LiCGC-gated FETs. With this technique values of $\approx$20 and $\approx$50 cm^2 V^{-1} S^{-1} electrons and hole mobilities were obtained, respectively.[51] We note that the discrepancy between the mobilities extracted from transfer characteristics and those obtained via Hall measurements may be partially attributed to contact resistance at the metal/semiconductor interface. In particular, limited carrier injection at the contacts can lead to an underestimation of the field-effect mobility extracted from transfer curves, compared to Hall measurements that probe intrinsic transport properties more directly.

A summary of the values obtained for μ, the SS, ON/OFF current ratios and V_{th} for 15 measured devices can be found in Figure S7 and Table S2 in the Supporting Information. For comparison, Table S2 (Supporting Information) also includes data from three state-of-the-art reports on both CVD-grown and exfoliated WSe_2 single layers. While those studies report higher hole mobilities, the ON/OFF ratios are comparable or lower, and ambipolar behavior is not consistently demonstrated. Additionally, the here reported subthreshold swings are higher overall, highlighting the effective gate control and balanced performance achieved in our devices.

For reference, standard Si/SiO_x bottom gate, top contact FETs were fabricated. Highly doped p++ type Si/SiO_x (300 nm oxide layer) substrates served both as supporting substrate and as gate. Transferred 1L-WSe_2 used as channel material was stacked with Cr/Au contacts with the same channel dimensions as LiCGC-gated substrates (20 × 50 µm). Representative output and transfer curves are displayed in Figure S8 (Supporting Information). While functioning ambipolar Si/SiO_x-gated devices were archived, the saturation current (I_{sat}) was typically two orders of magnitude smaller (at 40× higher V_{gs} and 4× higher V_{ds}) compared to LiCGC-gated devices. Furthermore, ON/OFF ratios were typically $\sim 10^2$, which corresponds to ratios six to seven orders of magnitudes lower at gate voltages 10× higher than their LiCGC-gated counterparts. These results clearly underscore the advantage of the solid-state electrolyte gating technique.

Figure 3f displays in semi-logarithmic scale a transfer curve measured at $V_{ds} = 0.05$ V. The red and blue regions in the plot indicate where the electron and hole current occur, respectively. At low drain voltages such as this, ionic-gate spectroscopy can be performed to directly extract the E_g of a semiconductor from the transfer curve of the transistor.[51,65] The E_g is given by the voltage difference between the electron and hole current onsets, which are determined by the current cutoff threshold voltages of the electron and hole currents, respectively.[65] This is expressed as $E_g = e(V_{th}^e - V_{th}^h)$, with V_{th}^e and V_{th}^h representing the threshold voltages for the electron and hole currents. For ionic-gate spectroscopy I_{ds} is plotted against V_{ref}, the potential measured by a reference electrode. This electrode measures the potential at the top of the LiCGC substrate near the channel, hence the voltage the channel material is experiencing, rather than the to the bottom applied voltage V_g. In an ideal device, when the gate electrode undergoes a sweep of ΔV_g, then the measured sweep at the reference ΔV_{ref} should equal ΔV_g. This can be used to monitor the gate efficiency, defined as $\Delta V_{ref}/\Delta V_g$, where the value of 1 indicates ideal gating efficiency.[51,65] If $\Delta V_{ref}/\Delta V_g$ is < 1, the extracted E_g from the I_{ds}-V_g curve would not be accurate. Most of the investigated devices show $\Delta V_{ref}/\Delta V_g = 0.99$, indicating close to 100% gate efficiency. However, for more accuracy, I_{ds} is plotted against V_{ref} to extract E_g from the transfer curve. The measured value for E_g is 1.83 eV. This is in excellent agreement with the value for E_g calculated employing the expanded Schottky-Mott rule (see Formula 1). Figure S9 (Supporting Information) provides additional transfer curves used for E_g-extraction, along with corresponding plots of V_g versus V_{ref}, showing their linear relationship. Additionally, Figure S10 (Supporting Information) presents a representative transfer curve on a linear scale, illustrating the E_g extraction by interpolating the threshold voltages for electron and hole conduction.

3. Conclusion

We have demonstrated the exfoliation and transfer of centimeter-sized 1L-WSe_2, where the dimensions and crystallinity of the 1Ls are solely limited by the parent crystal. We achieved this by employing a gold-mediated, thermally activated exfoliation process with template stripped exfoliation substrates combined with high-quality WSe_2 parent crystals. This approach yields ultra-smooth Au substrates, facilitating ideal vdW interaction between the Au template and the outer layer of the TMDC. Reaching 1L-areas up to 20 mm^2, we provide an accessible and reliable method for producing large-area, high-quality WSe_2, with minimal multilayer contamination. Furthermore, we employed a gold-assisted, polymer-free transfer procedure, which transferred our 1Ls without identifiable loss in size or quality.

The quality of the exfoliated and transferred 1L-WSe_2 was confirmed through comprehensive characterization techniques, including Raman spectroscopy, PL measurements, XPS, UPS and electronic transport measurements. For the electric transport measurements, we fabricated FETs on solid-state electrolyte gating LiCGC substrates and set a new precedence for SS and ON/OFF current ratios for this device architecture. Furthermore, we demonstrate the possibility for ionic gate spectroscopy employing LiCGC substrates as gating material, which allows to extract the E_g of the channel material directly from the transfer curves of the FETs. With this device architecture a steep SS as low as 30 and 50 mV dec^{-1}, maximum mobility of 16 and 18 $cm^2 V^{-1} s^{-1}$, ON/OFF current ratios of $\approx 10^8$ and $\approx 10^9$ for electron and hole currents, respectively, were achieved, putting these devices on the top rank of 1L-WSe_2 devices in literature. The reliability of the material and device performance is demonstrated over a set of 15 fabricated devices.

The presented technique can be easily implemented in laboratories without needing expensive equipment like CVD. The availability of large-area, high-quality single layer TMDCs is key to advancing research and the development of these materials for electronics. Understanding their electrical properties enables the integration of 2D materials into semiconductor technologies, leading to simpler fabrication, further device miniaturization, and new nanoscale applications. Additionally, efficient large-scale layer transfer without losing size or quality of the 1L-TMDC could refocus research on optimizing large, high-quality bulk crystal growth. If the size and crystallinity of the exfoliated monolayer depend on the parent crystal, large-area 1L-TMDCs could be exfoliated and transferred, much like in silicon technology, where wafers are produced from bulk crystals.

4. Experimental Section

Sample Cleaning: All substrates were cleaned in an ultrasonic bath in deionized water, acetone, IPA, then dried under nitrogen flow. Afterward the substrates were plasma cleaned (0.35 mbar O_2, 5 min, Diener Plasma cleaner) to remove hydrocarbon contamination.

Metal Exfoliation Substrates: The fabrication of ultra-smooth gold surfaces needed for the metal-assisted exfoliation followed the procedure as previously reported.[35,44] 100 nm Au and 900 nm Cu were deposited on highly polished Si wafers (Sigert Wafer, <100>, 525 µm thickness) via physical vapor deposition (≈ 1.0 Å s^{-1} at 10^{-6} mbar). Glass substrates were fixed onto the metal coated Si wafers with UV-curable epoxy resin (Osilla Encapsulation Epoxy S132) and UV cured (254 and 365 nm, 2 h).

Metal-Assisted Exfoliation: WSe_2 (2D semiconductors, synthetic crystal) was cleaved with heat resistant Kapton tape and transferred onto freshly template-stripped metal substrate. After annealing (200 °C, 120 s) the Kapton tape was removed from the substrate, leaving 1L-WSe_2 on the exfoliation substrate.

Metal-Assisted Transfer: Exfoliated 1L-WSe_2 on the exfoliation substrate was placed on aqueous $FeCl_3$ (33 wt.%) solution. The sample remained on the etchant until the Au/WSe_2 foil floated freely on top (12 h). The Au/WSe_2 foil was removed from the etchant with a clean glass slide and transferred onto DI water. This process was repeated two times to remove etchant residue. Subsequently, the foil was transferred into IPA, where the reduced surface tension allows the foil to sink and be flipped. The flipped foil can be fished out with the target substrate or carefully pushed on to the target substrate in the solution and the solution removed with a pipette. Afterward, the sample is dried (1 h) before an annealing step (150 °C, 30 min). Au is etched for 30 min with aqueous KI/I_2 etchant (Sigma Aldrich, "Au etchant, standard"). To remove etchant residue the sample was rinsed with acetone and IPA, respectively.

Scanning Force Measurements: SFM was performed in air using a Brunker Dimension Icon using PeakForce Tapping with a PFQNE-AL tip (Bruker).

Raman and Photoluminescence Measurements: Raman and PL spectroscopy were performed using a confocal microscope setup (Horiba Ldt.) with a 532 nm Laser excitation source and 20× objective (≈ 3 µm laser spot size) using a 1800 and 600 L mm^{-1} grating, respectively. The measurements were performed in ambient conditions.

X-Ray and Ultraviolet Photoelectron Spectroscopy: The XPS and UPS measurements were conducted in a Prevac ultra-high vacuum system (base pressure $1 \cdot 10^{-10}$ mbar), including an EA15 hemispherical analyzer, the Al k-alpha radiation of a monochromated X-ray source and a monochromated Helium discharge lamp using the HeI alpha emission line. The employed experimental energy resolutions were ca. 300 meV in XPS and 60 meV in UPS.

Photolithography: Photolithography was performed using a maskless aligner (Heidelberg µMLA, 390 nm LED light source). LOR and ECI3007 resists (MicroChemicals) were subsequently spin coated (4000 rpm, 180 s) and heat treated (180 and 100 °C, respectively). After the lithography process (115 mJ/-9 def), AZ 726 MIF (MicroChemicals) was used as developer (90 s). Subsequently, deionized water was used to stop the developing process and rinse the substrate. The remover was rem-700 (MicroChemicals). All lithography steps were performed in a clean room with controlled humidity and temperature. A schematic illustration of the photolithography process is displayed in Figure S13 in the Supporting information.

LiCGC-Gated FETs: LICGC AG-01 polished substrates were purchased from OHARA as 25.4×25.4 mm squared and 150 µm thick substrates with polished top and bottom surfaces. One side of the substrates (referred to as the top side from here on) was covered with a protective polymethylmethacrylat (PMMA) layer. On the other side (referred to as the bottom side from here on) a Cr(6 nm)/Au(50 nm) layer, serving as gate contact, was deposited via thermal evaporation. After the PMMA was removed from the top side, alignment marks were fabricated by employing photolithography followed by the thermal evaporation of Cr(6 nm)/Au(50 nm). The substrate was then cut into 8.5 × 8.5 mm pieces employing a wafer cutter. 1L-WSe_2 were transferred via metal-assisted transfer (as described above). The color code of 1L-WSe_2 on the ceramic under polarized microscope imaging was confirmed via PL and Raman measurements. Excessive 1L-WSe_2 was removed by etching (0.35 mbar O_2, 5 min, Diener Plasma cleaner) employing photolithography. The extension and source and drain contacts (EC and SDC, respectively) were fabricated by two steps of photolithography method and subsequent oxide/metal evaporation. In the first step Al_2O_3/SiO_x/Cr/Au (10/50/40 nm) was thermally evaporated following the first step of photolithography. In the second step Pt/Ag (10/100 nm) was evaporated overlaying the Al_2O_3/SiO_x/Cr/Au layer and WSe_2 to create the contact between the EC and the SDC and the WSe_2 channel.

Si/SiO_x-Gated FETs: Si-gated devices were prepared on transferred 1L-WSe_2 on highly doped p++ type Si/SiO_x (300 nm oxide layer) substrates. The source and drain contacts were fabricated by thermal evaporation (≈1.0 Å s^{-1} at 10^{-6} mbar) of Cr(6 nm)/Au(50 nm) following photolithography method. Subsequently, a second cycle of photolithography was used for etching excessive single-layer WSe_2 around the channel regions using oxygen plasma (0.35 mbar O_2, 5 min, Diener Plasma cleaner).

Impedance Measurements: The measurements were conducted using a Solartron Analytical ModuLab XM system, comprising the XM MAT 1 MHz module, XM MFRA 1 MHz module, and XM MHV 100 module. The device was biased at a constant DC voltage of 1 V. An AC voltage with an amplitude of 0.1 V rms was superimposed to perform the impedance spectroscopy. The frequency sweep ranged from 1 MHz to 0.1 Hz, utilizing 10 data points per decade. The collected impedance spectra were fitted using an equivalent circuit model to extract the capacitance values.

Electronic Transport Measurements: All measurements were performed under inert nitrogen atmosphere. Electrical connections were made using a MPS150 probe station (Cascade) and the device characterization

performed using a Keithley 4200A-SCS parameter analyzer, equipped with four source-measure units (4200-SMU).

Statical Analysis: SFM and KPFM images were processed with the Gwyddion software. For UPS and PL measurements the Igor Pro 9 software from wavemetrics was used. The designs for photolithography were created and registered using optical microscope images in the AutoCAD software. For the electrical transport measurements SweepMe! Software was employed.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

ambipolar, exfoliation, FET, LiCGC, TMDC, WSe_2

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