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CMOS back-end-of-line integration of bilayer ferroelectric tunnel junction in 1-transistor-1-capacitor circuit

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ABSTRACT

Ferroelectric tunnel junction (FTJ) devices based on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ (HZO) have recently gained significant interest as CMOS back-end-of-line integrable low power non-volatile memories for neuromorphic computing applications. In this paper, we demonstrate integration of metal-ferroelectric-dielectric-metal bilayer FTJ devices in the back-end-of-line of a 180 nm CMOS technology chip. We present electrical characteristics of the integrated FTJ devices, including the polarization switching and resistance switching behavior with an ON/OFF current ratio of ~ 18, and an ON current density of ~ 24.5 μA/cm^2 at a read voltage of 1.8 V. Furthermore, we also demonstrate a 1-transistor-1-capacitor (1T1C) circuit by connecting a back-end FTJ device with a front-end nMOS transistor, which amplifies the ON current of the FTJ device by 2.6 times. Thus, we show the basic building block for the integration of HZO-based FTJ devices for neuromorphic applications.

1. Introduction

The report of ferroelectricity in hafnium oxide in 2011 was a significant breakthrough in ferroelectrics [1,2]. It opened up new possibilities for the integration of ferroelectric (FE) non-volatile memory devices with CMOS technology [3]. Among the different non-volatile memory technologies, ferroelectric tunnel junction (FTJ) devices have attracted significant attention due to their potential as ultra-low power synaptic devices for neuromorphic computing [4].

A conventional FTJ device consists of a ferroelectric layer sandwiched between two dissimilar metal electrodes. The ferroelectric layer is the tunneling layer, and the tunneling current depends on the direction of its polarization. To obtain a reasonable tunneling current, an ultra-thin ferroelectric layer (typically 1–4 nm) is necessary [5]. Although there have been reports of ultra-thin $Hf_{0.5}Zr_{0.5}O_2$ (HZO) layers (~1 nm) with good remnant polarization recently, it is still quite challenging to reliably obtain such layers [6,7]. An alternative bilayer stack consisting of metal-ferroelectric-dielectric-metal (M-FE-DE-M) allows to obtain a reasonable ON/OFF ratio while utilizing a thick (typically 8–12 nm) HZO layer [8,9]. In this case, the dielectric layer (typically 1 – 4 nm) is the tunneling layer [9,10], and the polarization direction of the ferroelectric layer leads to different band bending in the ferroelectric-dielectric barriers, resulting in different tunneling currents [11,12]. The fast switching and long-term stability of the ferroelectric polarization make these devices attractive for high-speed memory applications [13,14]. Moreover, the low crystallization temperature of HZO (~400°C) enables these devices to be integrated into the CMOS back-end-of-line (BEOL) [10], which is an essential step towards the implementation of FTJ devices as embedded non-volatile memory in edge computing. Recently, TiN / HZO (5 nm) / TiN and TiN/Al_2O_3 (2 nm) / HZO (5 nm)/TiN FTJ devices of 100 × 100 nm^2 dimensions have been implemented on top of a 300 mm wafer platform [15]. However, this work demonstrated standalone FTJ devices in BEOL process flow with only metallization layers on Si substrate and no underlying CMOS transistors. In view of future neuromorphic circuits based on hybrid CMOS/FTJ devices [16,17], it is essential to study the integration of FTJ with underlying front-end CMOS transistors. A challenge is that the required annealing temperature for HZO crystallization is very close to

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the upper thermal budget allowed for BEOL processing (400–450°C); therefore, the integrity of the transistors after the FTJ fabrication has to be assessed. Bilayer FTJ devices typically have low ON current density (10 – 25 μA/cm^2 [4,13,18,19]) and require some level of current amplification by the transistors in neuromorphic circuits. A 2-transistor-1-capacitor (2T1C) circuit was proposed in [20] to amplify the current through the FTJ (and in [21] for FeRAM). A 2T1C circuit, as shown in Fig. 1, consists of a write transistor whose drain is connected to the gate of a read transistor. One terminal of the capacitor (or FTJ) is connected to this common gate-drain node. This node is an electrically floating node. A 1T1C sub-circuit in the 2T1C connection is highlighted in Fig. 1. This sub-circuit forms the read path for the FTJ and performs the function of amplifying the current of the FTJ. This sub-circuit topology allows a lower area for the memory cell compared to traditional DRAM-like 1T1C or 1T1R [22], where the capacitor or FTJ is connected to the drain of the access transistor and read through the same without any amplification. The current amplification in 1T1C read sub-circuit in Fig. 1 is achieved by charging of the floating gate of the read transistor (during read operation), which then converts to an exponential increase in drain current as the floating gate voltage builds up to threshold voltage of the transistor. For the highest amplification, the voltage build up on the floating gate of read transistor should reach the maximum transconductance bias point. While there has been an experimental demonstration of the 2T1C cell concept in [21] (which includes the 1T1C read sub-circuit for amplification), it was performed by connecting ferroelectric capacitor with discrete transistors on a PCB and only featured destructive readout, as in DRAM/FeRAM. In this work, we demonstrate the 1T1C read sub-circuit of the 2T1C by integrating the FTJ device on top of a commercial CMOS wafer and connecting the FTJ to the gate of a front-end-of-line nMOS transistor, which serves to amplify the output current of the FTJ. We performed electrical measurements to show current amplification in the 1T1C read sub-circuit. Thus, we experimentally show one of the key building block for back-end-of-line integration of FTJ devices.

2. Experimental details

In this work, we integrate W-Al_2O_3-HZO-TiN FTJ devices in the back-end-of-line of a 180 nm CMOS chip from a commercial foundry (XFAB) and connect them with nMOS transistors situated in the front-end-of-line of the chip to demonstrate a 1T1C circuit. Stand-alone FTJs (not connected to a transistor) characterization is carried out to assess their performance after on chip integration. The transistors in the front-end are characterized before and after the FTJ integration to assess the potential detrimental impact of the BEOL integration processes, especially of the HZO annealing step. 1T1C circuit measurements (made by connecting the bottom electrode of the back-end-of-line FTJ device to the gate of the front-end-of-line nMOS transistor) are performed to demonstrate FTJ current amplification. This work shows the realization of the basic building block for BEOL integrated FTJ non-volatile memory technology for neuromorphic computing and embedded memory applications.

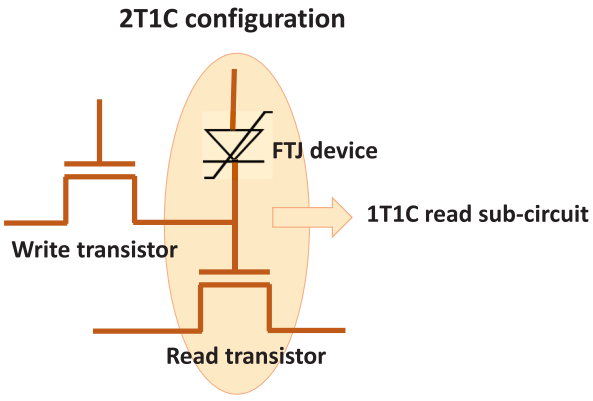

Fig. 1. Schematic illustration of a 1T1C circuit, shown as a sub-cell of the conventional 2T1C configuration.

Bilayer HZO/Al_2O_3 FTJ devices with bottom tungsten (W) and top titanium nitride (TiN) electrodes were fabricated above W via on an X-FAB 180 nm CMOS chip as shown in Fig. 2. The CMOS wafer was cut into dies of 2 x 2 cm^2 area. As the chip was obtained from the foundry after 3rd via level (generally known as V3), a 10 nm Al_2O_3 layer was first deposited to electrically isolate the bottom FTJ electrode from vias below. Then, 30 nm-thick W bottom electrodes were patterned by a lift-off process consisting of direct laser writing lithography (Heidelberg Instruments DWL 66+) and W deposition by sputtering at room temperature. Next, 3 nm Al_2O_3 and 10 nm HZO amorphous films were deposited by atomic layer deposition (ALD) at 250°C using trimethyl aluminium (TMA) precursor for Al_2O_3, Tetrakis(ethylmethylamido)-Hafnium (TEMA-Hf) and Tetrakis(ethylmethylamido)-Zirconium (TEMA-Zr) precursors for HZO respectively, with water as co-reactant for both layers. TiN top metal electrodes (30 nm) with W capping (30 nm) were patterned by lift-off (direct laser lithography and metal deposition by sputtering at room temperature). The die was annealed using rapid thermal processing (RTP) at 400 °C for 180 s in N_2 for crystallizing the HZO layer into the polar orthorhombic phase. Finally, the bottom contact electrodes were opened by etching the Al_2O_3/HZO layers using BCl_3-based reactive-ion etching (RIE). The devices have dimension of 75 x 75 μm^2. In order to connect the FTJ to the transistors below in the front-end-of-line, a W line was fabricated by lift-off, linking the bottom electrode of the FTJ to the via (in V3 layer) connected all the way down to the gate contacts of the transistors. In this work, the FTJs were connected to an nMOS transistor to complete a 1T1C circuit. Several stand-alone FTJ devices not connected to a transistor were also fabricated on the same chip. I-V and P-V measurements were carried out using a Radiant Multiferroic II tester with a triangular voltage of ± 5.0 V applied on the top electrode while grounding the bottom electrode. The wake-up cycling was performed with square pulses of ± 5.0 V amplitude and 1 ms pulse width [14]. The ON and OFF state currents were measured using a DC read voltage of + 1.8 V (averaged over 500 ms). Reset and Set operations were carried out with square pulses of −5.0 V and + 5.0 V amplitude, respectively, and 0.5 ms pulse width. The quasi-static I-V read measurements for both the stand-alone FTJ devices and the 1T-1C circuits were conducted using the B1500 semiconductor device parameter analyzer.

3. Results and discussion

The switching I-V measurements of the W-Al_2O_3-HZO-TiN FTJ device at pristine, 1000 and 2000 cycles, are shown in Fig. 3(a). In the pristine state, the coercive voltage peak in the positive polarity (HZO polarization towards Al_2O_3, ON state) is at ~ 4.0 V whereas in the negative polarity (HZO polarization away from Al_2O_3, OFF state) the peak is not very distinct. Instead, in the negative polarity, the coercive voltage distribution is very broad. After 1000 cycles, the coercive voltage distribution in positive polarity narrows down leading to an increase in the peak current. The positive coercive voltage peak does not change much (~4.1 V). For the negative polarity, the coercive voltage distribution decreases, the switching peak becomes more evident and is located at ~ -3.0 V. After 2000 cycles, the switching peaks narrows even more and the switching peaks corresponding to positive and negative polarities are located at ~ 4.1 V and ~ -2.7 V respectively. The remnant polarization increases from pristine to 2000 cycles indicating ferroelectric wake-up (Fig. 3(b)). In order to extract the remnant polarization without dielectric and leakage contribution, PUND measurements were performed (not shown here), and the remnant polarization P_R is ~ 12 μC/cm^2 after 2000 cycles.

The pulse sequence used for measuring the OFF and ON currents is displayed in Fig. 4(a). In Fig. 4(b), the evolution of read currents

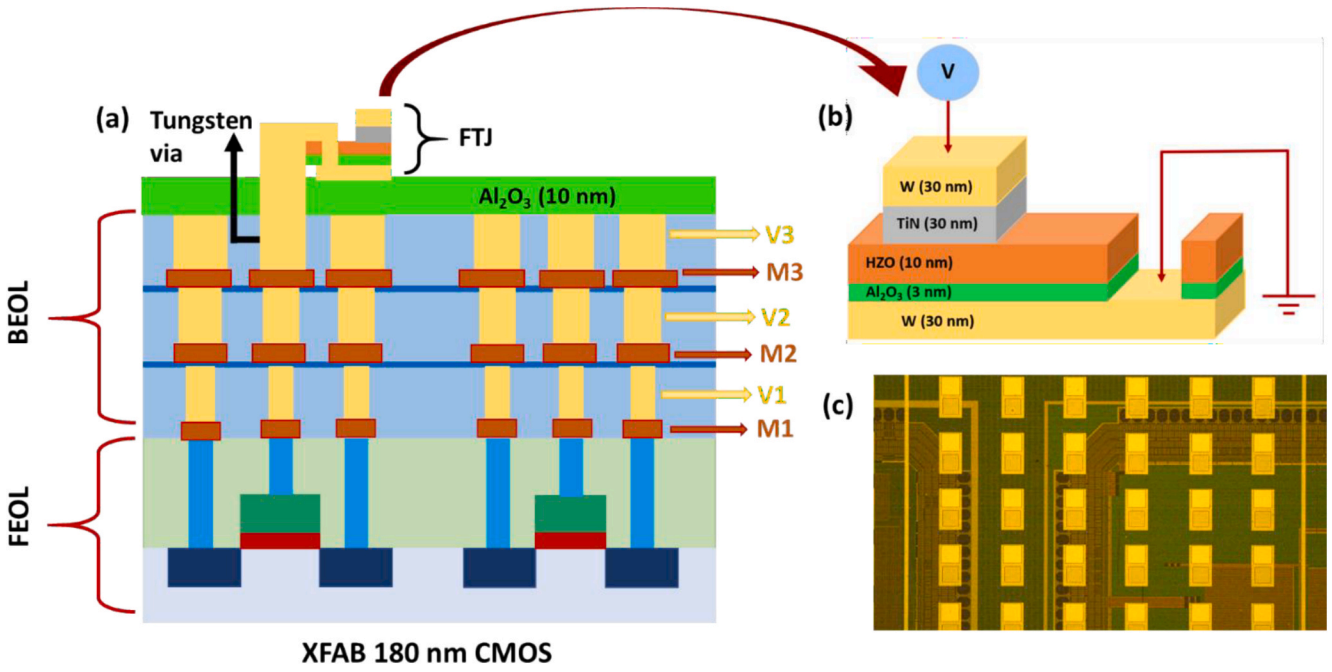

Fig. 2. (a) Cross section schematic of the CMOS BEOL stack and integrated FTJ at V3 level; (b) Schematic of FTJ stack; (c) Top view optical microscopy image of the FTJ devices integrated on V3 level. Bright yellow areas are FTJ devices. Metal lines (brown or dull yellow) from BEOL layers below are also visible outside FTJ device area.

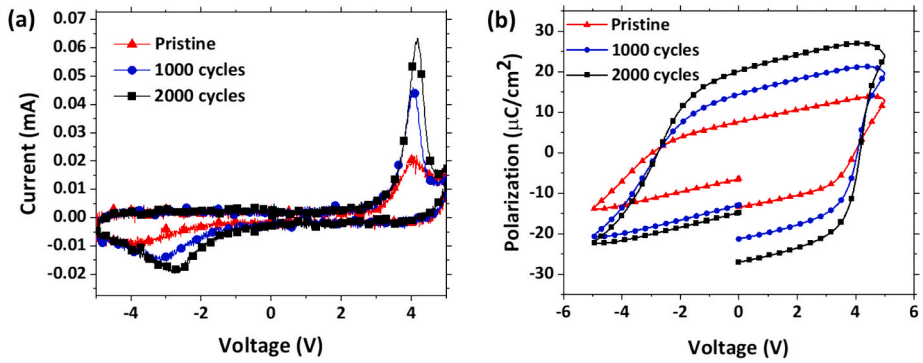

Fig. 3. (a) I-V curves for pristine state and after 1000 and 2000 cycles for the FTJ device of 75 × 75 μm^2 which was later connected to the nMOS transistor gate. (b) P-V hysteresis loops for pristine state and after 1000 and 2000 cycles from the same device. The wake-up cycling was performed with square pulses of ± 5 V and 1 ms width.

corresponding to the Reset (OFF state) and Set (ON state) states of a FTJ device are shown for two devices of different dimensions. After the wake-up of 2000 cycles, the FTJ device exhibits an OFF current of about 0.07nA (1.24 μA/cm^2) and an ON current of approximately 1.38nA (24.5 μA/cm^2). The evolution of ON/OFF ratio from pristine to 2000 cycles for device A (6000 cycles for device B) is shown in Fig. 4(c). The ON/OFF ratio increases from 6 in the pristine state to about 18 after 2000 cycles (for device A). These results are comparable with our typical baseline FTJ devices fabricated on Si substrate [10,14] where the ON/OFF ratio is 5–35 and the ON current density is 20–30 μA/cm^2. Thus, these FTJ devices fabricated in the BEOL of the XFAB CMOS chip show comparable performance as those on Si substrate. Retention characteristics from an equivalent device stack fabricated on Si wafer is shown in Fig. 4(d). The stack shows a separation between ON state and OFF state up until 10^5 s. After identifying and characterizing device A in stand-alone condition, it is then connected to the FEOL transistor gate by lift off of metal conduction line of width 25 μm, connecting the bottom electrode of the FTJ and the via PAD corresponding to the gate of the transistor.

During the fabrication of the FTJ devices, the crystallization of HZO to its ferroelectric orthorhombic phase is a critical step, which we perform at a temperature of 400 °C (under N_2, for 180 s). It is essential that the silicon transistors of the CMOS chip are not damaged during this process. As shown in Figs. 5(a) and 5(b) the drain current (I_D) versus gate voltage (V_G) (transfer characteristics) and the drain current (I_D) versus drain voltage (V_D) (output characteristics) before and after the fabrication of the FTJ devices overlap very well, indicating that the fabrication process has not altered the transistor properties. The transistor shown in Fig. 5 is nMOS with gate length (L_g) = 300 nm and width = 1 μm.

While the FTJ device has potential for low power consumption due to voltage driven switching mechanism, the high resistance may pose a challenge in circuit implementations. It will be necessary to have higher read current, which can be achieved by combining the FTJ with a nMOS transistor in a common source amplifier like configuration. This is demonstrated here by connecting the bottom electrode of a FTJ with the gate of a nMOS transistor to form a 1T1C circuit as shown in the schematic in Fig. 6(a). The 1T1C circuit is a sub-circuit of 2T1C [20], which

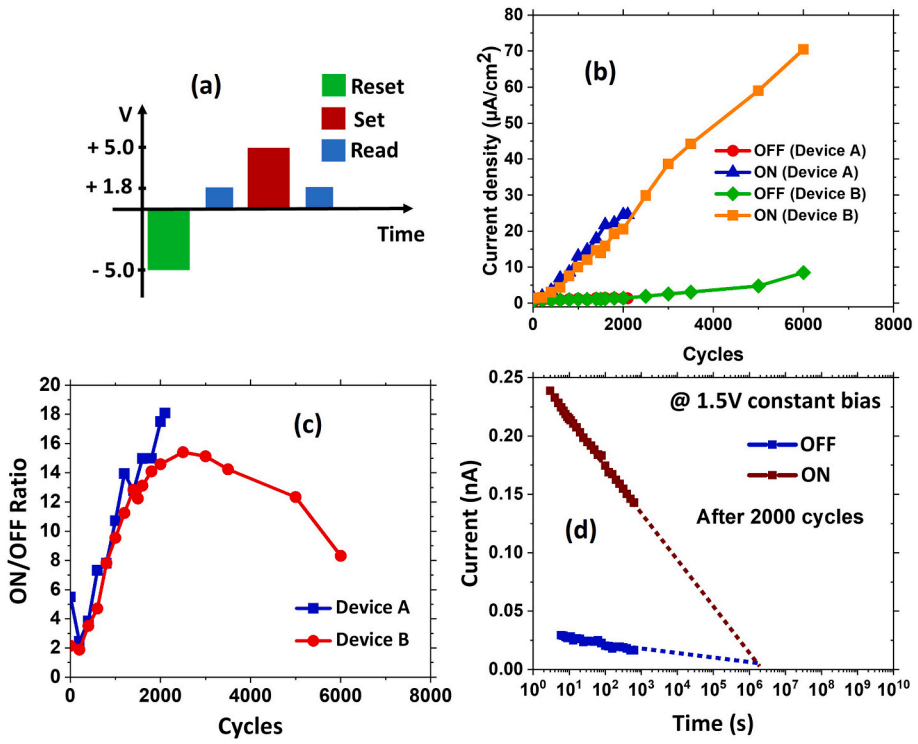

Fig. 4. (a) The pulse sequence used for the Reset, Set and Read operations. (b) Evolution of read current densities in the OFF and ON states (measured at 1.8 V read voltage) as a function of wake-up cycling for the FTJ devices A and B. Device A has a dimension of 75 × 75 μm^2 and was later connected to the nMOS transistor gate. Device B has a dimension of 100 × 100 μm^2. (c) Corresponding ON/OFF ratio extracted from (b) for devices A and B. (d) Retention characteristics measured on an equivalent stack fabricated on a Si wafer platform performed after wake up of 2000 cycles with a constant voltage bias of 1.5 V.

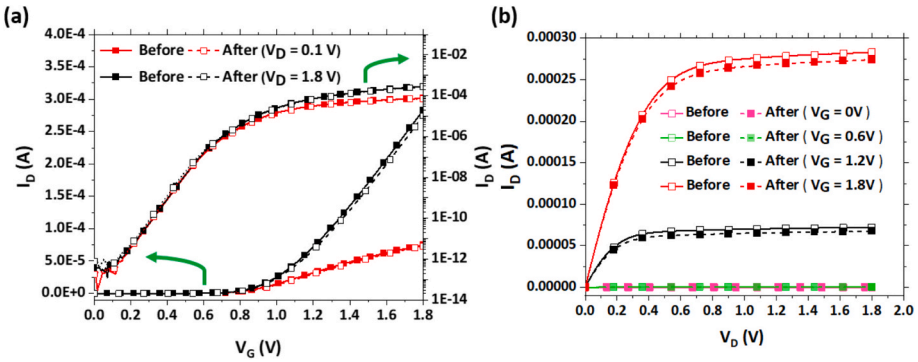

Fig. 5. (a) Drain current (I_D) as a function of gate voltage (V_G) (transfer characteristic) and (b) Drain current (I_D) as a function of drain voltage (V_D) (output characteristics) characteristics of a nMOS transistor, before and after the fabrication of the ferroelectric tunnel junction (FTJ) devices on top of the CMOS chip. This transistor (situated in the front-end-of-line of the chip) is connected to one FTJ to form a 1T1C circuit.

allows amplification of the FTJ current by the connected transistor. The top and bottom electrodes of the FTJ connected to the transistor have large pads to be able to measure the FTJ independently without the transistor. This is the standalone FTJ measurement as shown in Fig. 6(b). This configuration is also used to Set and Reset the FTJ prior to performing read measurements through the transistor. During standalone measurements of the FTJ, the bottom electrode is always grounded in order not to damage the transistor. The FTJ device is switched to OFF and ON states by performing Reset (square pulse, −5.0 V, 0.5 ms) and Set (square pulse, +5.0 V, 0.5 ms) operations respectively, by applying a voltage pulse on the FTJ top electrode using the ferroelectric tester. During the Set or Reset operation, both the source and drain of the transistor are kept floating. After the Reset or Set operation, the ferroelectric tester is disconnected. Once the FTJ device is either Reset (OFF state) or Set (ON state), the read measurement through the transistor (1T1C circuit) is performed by sweeping the read voltage (V_{read}) from 0 to 2.0 V on the FTJ top electrode (see Fig. 6(b)). At the same time, a constant drain voltage (V_D) of 1.8 V is applied on the drain of the transistor and the source terminal is grounded (as this is 180 nm CMOS technology, the supply drain voltage needed for the transistor is 1.8 V). When sweeping V_{read}, the current flowing through the top electrode charges the gate capacitor of the transistor. This leads to an increase of the gate-to-source voltage. The larger the current through the FTJ, the larger the voltage increase at the gate node of the transistor. When the FTJ is in OFF state, the current through the device is low and the effective voltage on the gate is low, whereas when the FTJ is in ON state, the current through the FTJ is high and thus the voltage at the gate node is high. A high gate-to-source voltage leads to a high current flow between the drain and source of the transistor. As the drain current of the transistor exponentially increases with gate-source voltage (see Fig. 5(a)), the FTJ

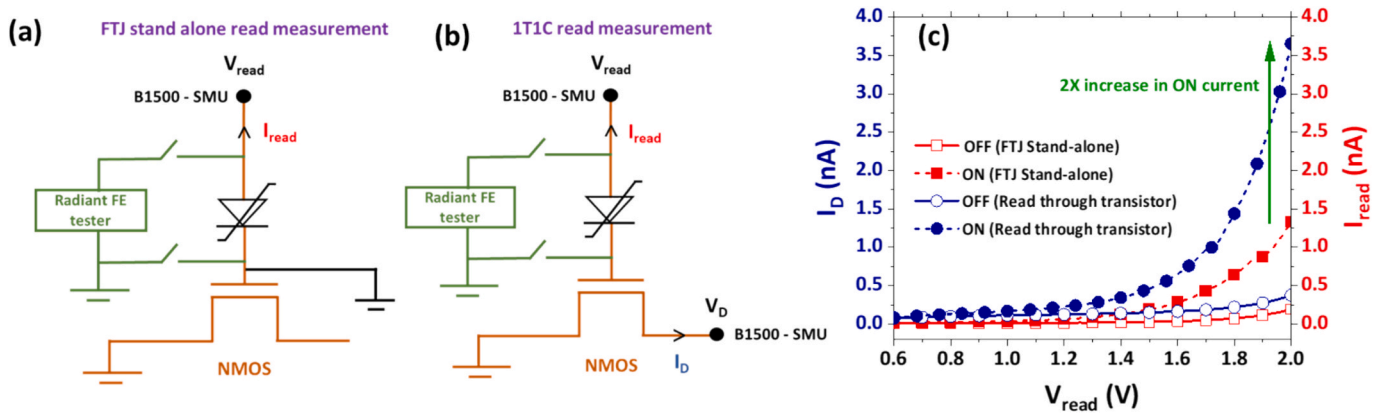

Fig. 6. (a) Setup schematic for measuring the OFF and ON quasi-static read current for stand-alone FTJ configuration. (b) Setup schematic for measuring the OFF and ON quasi-static read current through the 1T1C configuration (c) Quasi-static measurement of the OFF and ON state currents as a function of read voltage for the stand-alone FTJ (in red) and for the FTJ read through the 1T1C circuit (in blue).

current is amplified and is measured as drain current of the transistor. The stand-alone FTJ read current measurement is carried out by sweeping the top-electrode voltage from 0 to 2.0 V, while grounding the bottom electrode (see Fig. 6(a)). In this case the V_D is zero (terminal not connected to B1500-SMU) and the source is not grounded.

The comparison between the OFF and ON state quasi-static read currents, measured through the 1T1C circuit and for the stand-alone FTJ, is shown in Fig. 6(c). The standalone measurement yields an OFF current of ~ 0.19nA (3.37 μA/cm^2) and an ON current of ~ 1.32nA (23.4 μA/cm^2) at 2.0 V read voltage, resulting in an ON/OFF ratio of ~ 7. For the 1T1C circuit, the OFF current is ~ 0.37nA (6.57 μA/cm^2) and the ON current is ~ 3.65nA (64.8 μA/cm^2) at 2.0 V read voltage, hence showing a current amplification of 2.6 times (with an improved ON/OFF ratio of ~ 10). The amplification of current demonstrates the feasibility of a basic FTJ-CMOS hybrid circuit integrated on CMOS chip [16,20,21].

The current amplification will be highest if the floating node (the gate of the read transistor in Fig. 6) is raised to voltage that leads to maximum transconductance in the transistor. For the nMOS we have measured, this is about 1 V. If one considers the voltage drop across the FTJ and the nMOS gate capacitor, at this voltage on nMOS gate, the FTJ will have about 1 V across it. Owing to the exponential dependence of the FTJ current on voltage across it (due to tunneling conduction), the current drops significantly. From Fig. 6 it can be observed that, with 1 V across the FTJ, its ON current will be about 0.03nA. Hence, the current flow to charge the nMOS gate capacitor is negligible. In fact, the ON current of the FTJ drops to about 0.2–0.3 nA at around 1.5–1.6 V. We can assume that below this level of ON current, the gate capacitor will not charge much during read measurement. So, the effective voltage the read transistor gate is raised to is ~ 0.4–0.5 V. From Fig. 5 the drain current of nMOS for this range of gate voltage is about 2–10 nA. This is the same range of amplified current we observe in Fig. 6(c). In order to further increase the amplified current, either the read nMOS width has to be increased or its threshold voltage has to be lowered. Utilizing read transistors with threshold voltage around 0.4 V would provide high amplification.

An additional aspect is the sizing of the FTJ and the transistor. In our case, the FTJ has an area of 75 x 75 μm^2 and the transistor has an area of 0.3 x 1 μm^2. So, the cell foot print is the same as the FTJ one owing to its larger size. A large FTJ was chosen to minimize fabrication risks in post-processing in the laboratory on a foundry fabricated wafer. However, the cell scaling limit is governed by the FTJ ON current density and targeted read time. Since the 1T1C read circuit with FTJ can be considered as a series RC circuit, the read time is roughly the R_{FTJ} x C_{OX} (C_{OX} – gate oxide capacitance). The resistance of the FTJ, R_{FTJ}, is inversely proportional to its area (A_{FTJ}). C_{OX} is directly proportional to nMOS area (A_{nMOS}). For a fixed read time target, the amplified current is directly proportional to A_{FTJ} and inversely to A_{nMOS}. Higher FTJ ON current density provides higher amplified current. Regarding the write operation, the presented circuit needs to have a write transistor as in a 2T1C circuit [21]. In this work, we have utilized external voltage source to perform the write operation.

A comparative analysis of the achieved ON current density against state-of-the-art bilayer FTJ devices is presented in Table 1. For FTJs with thicker ferroelectric layers, this work demonstrates the highest ON current density to date, to the best of our knowledge. While higher densities are reported, these typically occur in devices with thinner ferroelectric layers (≤3 nm) [23,24,25]. Attaining stable ferroelectricity in HZO films at such reduced thicknesses remains a substantial material and fabrication challenge, often compromising ferroelectric properties and increasing device variability. This study achieves a record ON current density of 64.8 μA/cm^2 in a 10 nm ferroelectric layer, enabled by 1 T1C circuit integration. We also have switching energy or energy per write of about 4.95 nJ (normalized to the device area, it is about 880 fJ/μm^2).

4. Conclusion

In summary, we integrated W-Al_2O_3-HZO-TiN bilayer FTJ devices into the CMOS back-end-of-line of a foundry chip and demonstrated a

Table 1
Comparison of ON current density for Various HZO-Based bilayer FTJ devices.

Reference	FTJ Structure	ON current density	ON/ OFF ratio
This work	W/ Al_2O_3/HZO(10 nm)/W Stand alone; 1T1C combined (non-destructive read)	23.4 μA/ cm^2;64.8 μA/ cm^2	18
Max et al. [13]	TiN/HZO (8 nm)/Al2O3/TiN	7.16 μA/cm^2	10
Shekhawat et al. [18]	p-Ge/Al_2O_3/HZO (8 nm)/TiN	17 μA/cm^2	14
Ryu et al. [4]	p-Si/HZO (12 nm)/Al_2O_3/Ti/Au	10.16 μA/cm^2	3
Bégon-Lours et al. [19]	TiN/TiO_2/HZO (4.5 nm)/TiN	1 μA/cm^2	2
Chu et al. [23]	TiN/HZO (3 nm)/Al_2O_3/Ni	10^8 μA/cm^2	6.4
Cheema et al. [24]	Si/SiO_2/$Hf_{0.8}Zr_{0.2}$ (1 nm)/W	10^7 μA/cm^2	200
Chouprik et.al. [25]	Si/SiOx/HZO (2.5 nm)/TiN	10^6 μA/cm^2	3
Sünbül et. al. [26]	Si/SiO_2(1 nm)/HZO(8 nm)/TiN/ poly-Si	3×10^3 μA/cm^2	6
Luo et al. [21]	2T1C FeRAM (TiN/HZO(10 nm)/ TiN) (destructive read)	4×10^3 μA/cm^2 **	100

** Transistor gate capacitance ~ 1 pF but area is not indicated. So, value estimated from FE capacitor area (5×5 μm^2).

1T1C circuit by connecting a FTJ in the back-end-of- line with a nMOS transistor in the front-end-of-line. The standalone FTJ devices exhibit a large ON/OFF ratio of 18 and an ON current density of 24.5 μA/cm^2. We demonstrate negligible impact of the FTJ integration process on the transistor characteristics. For FTJs connected to a transistor, an amplification of the ON current by 2.6 times is achieved. These results demonstrate the feasibility of integrating FTJ devices with CMOS technology for neuromorphic computing and embedded non-volatile memory applications.

CRediT authorship contribution statement

Keerthana Shajil Nair: Writing – review & editing, Writing – original draft, Visualization, Validation, Investigation. **Muhammad Hamid Raza:** Writing – review & editing, Investigation. **Catherine Dubourdieu:** Writing – original draft, Validation, Supervision, Project administration, Methodology, Investigation, Funding acquisition, Conceptualization. **Veeresh Deshpande:** Writing – original draft, Validation, Supervision, Project administration, Methodology, Investigation, Conceptualization.

Declaration of competing interest

The authors have no competing interest to disclose.

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Data availability

Data will be made available on request.

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