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Inkjet-Printed Metal Halide Perovskite Thin-Film Field-Effect Transistors

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ABSTRACT

Metal halide perovskites (MHPs) are promising semiconductor materials for thin-film field-effect transistors (FETs) due to their high charge carrier mobility and solution processability. Currently, MHP thin films for FETs are mostly fabricated by spin coating, a method limited by poor material utilization, non-uniformity, and scalability issues. In this study, inkjet-printing (IJP) is successfully introduced as a sustainable, additive technique for MHP thin-film FET fabrication. Spin-coated benchmark devices were first established as a performance reference achieving a mobility of 2.2 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 8×10^6. Two inkjet-based strategies are investigated: full-substrate printing and selective in-channel printing. With the full-substrate printing approach we could achieve 1.6 $cm^2\ V^{-1}\ s^{-1}$ and an on/off ratio of 2×10^6, which replicates the device performance of the spin coated reference devices. In-channel printing enables full patterning of the FET active region and significantly reduces material waste but suffers from reduced device performance due to the coffee ring effect. By scaling the printed area and effectively isolating the coffee ring, the adverse effects are successfully mitigated, enabling a substantial recovery of device performance. This study highlights the strong potential of IJP for the fabrication of MHP thin-film FETs and provides valuable insights into overcoming current challenges. Overall, the results demonstrate that IJP is a highly promising route toward the scalable production of fully printed, high-performance perovskite electronics.

1 | Introduction

Research into metal halide perovskites (MHPs) has gained momentum over the last decade, due to the astonishing progress seen in the field of optoelectronics, especially photovoltaics and light emitting diodes (LEDs). The power conversion efficiency of MHP solar cells has increased from 13.9 % in 2013 to 27 % in 2025 [1–4]. Analogously, MHP LEDs have exceeded an external quantum efficiency of 25 % for multiple colors across a wide range of the visible spectrum, even enabling dual color LEDs [5–10].

On the other hand, the progress in MHP-based thin-film field-effect transistors (FETs) has so far not seen the same success, even though the first MHP thin-film FETs were reported in 1999. The fact that the properties of MHPs include a theoretical charge carrier mobility of over 1000 $cm^2\ V^{-1}\ s^{-1}$ and long-range balanced carrier transport, should make them a viable choice for thin-film FETs for display applications [11–14]. However, devices often suffer from hysteresis as well as a low subthreshold swing and reproducibility [12]. More recently, the focus of research has shifted to Sn-based MHP thin-film FETs, because they show a significant decrease in hysteresis and a higher subthreshold swing in comparison to earlier devices, which used Pb-based MHPs [15–17]. Using the Sn perovskite $Cs(Sn_{0.9}Pb_{0.1})I_3$, Liu et al. reported a maximum charge carrier mobility of 55 $cm^2\ V^{-1}\ s^{-1}$, showing the promising capabilities of Sn-based MHPs [16].

Up to now MHP thin-film FETs are mostly fabricated via spin coating. Spin coating is a simple, reliable and proven deposition method for thin films on the laboratory scale. It takes advantage of the properties of MHPs over alternative semiconductor materials in being processable from solution, which enables sustainable low-temperature fabrication [18–21]. Low-temperature processes are energy efficient, as well as compatible with a wide variety of substrate materials, including temperature sensitive polymers, while still being compatible with classical substrates, such as metals or glass. In comparison, the mainly used materials for back-channel transistors today are Si and In—Ga—Zn—O, which require temperatures up to 450°C during the fabrication process. This makes them energy-intensive and unsuitable for most flexible, low-cost polymer substrates that cannot withstand such high temperatures [22, 23].

However, during spin coating the whole substrate is coated and most of the precursor solution is spun off the substrate, making it a wasteful method. In the case of an MHP thin-film FET, this means that the perovskite is deposited on the whole substrate area, while it is only really needed in the transistor channel. Therefore, more efficient additive deposition methods are highly desirable, especially for devices with very small active areas, such as FETs with a channel area in the square micrometer range. Inkjet-printing (IJP) is such a deposition method. The drop-on-demand (DOD) approach of IJP enables the accurate positioning of drops directly in the transistor channel, which minimizes waste, making it sustainable and efficient. IJP is already well established in industrial applications, due to its scalability, in-line integration and customizability, which enables flexible production, as well as a fast adaptation to changes [22, 23]. Furthermore, IJP has proven to be a reliably working deposition method for MHP solar cells as well as MHP LEDs [7, 24–29]. Yet, to the best of our knowledge IJP has not been used to fabricate MHP FETs.

In this work, we investigated the capabilities as well as challenges and limitations of IJP as a deposition method for MHP layers in thin-film FETs. On the basis of the results of Liu et al. [16]., we first established a benchmark using spin coating, against which the IJP devices were compared. We then successfully transferred the fabrication process to IJP, utilizing two different approaches, the "full-substrate" and "in-channel" approach, thereby investigating the impact of the size of the printed area on the performance of MHP thin-film FETs.

2 | Results and Discussion

2.1 | Spin-Coated Benchmark FETs

We first fabricated spin coated devices because as mentioned above spin coating is a simple and reliable method, which is almost exclusively used for the fabrication of MHP thin-film FETs in literature. The process of spin coating is shown in Figure 1a. A drop of precursor solution is deposited at the center of the substrate, which is then spun at a predefined speed to expel excess solution. Solvent evaporation during spinning initiates MHP crystallization. Subsequent annealing removes residual solvent and finalizes the crystal structure. Although only needed in the transistor channels, the entire substrate is coated with an MHP

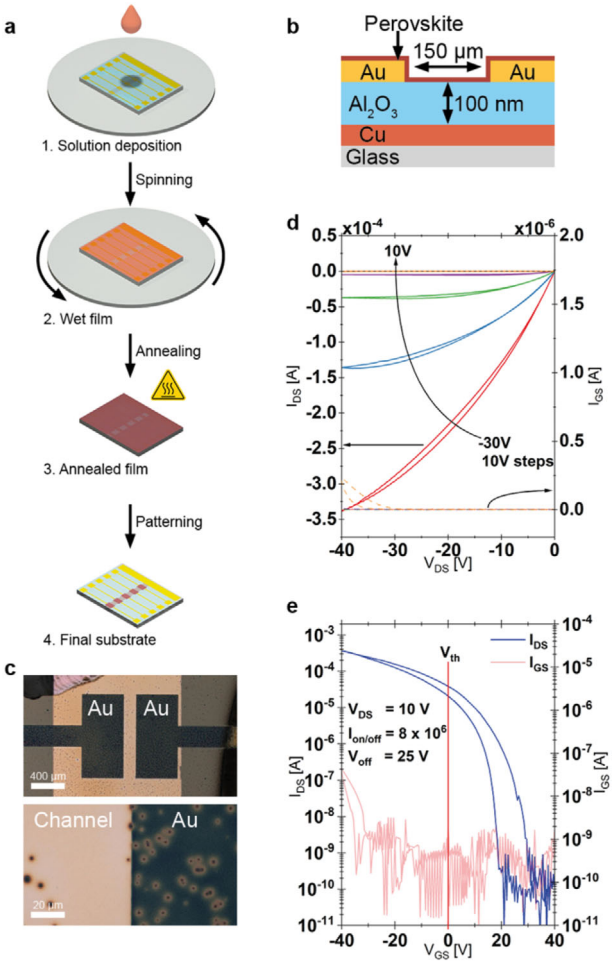

FIGURE 1 | (a) Spin coating process of MHP thin-film FETs, including the necessary patterning step. (b) Bottom gate, bottom contacts architecture of the MHP thin-film FETs, with 100 nm Al_2O_3 as dielectric material and 150 µm long channels. (c) Optical microscopy images of a MHP thin-film FET with the complete source and drain contacts (top) and zoom-in on the edge between the channel and a contact (bottom). (d) Output and (e) transfer characteristics of a spin coated MHP thin-film FET with almost no hysteresis and an on/off ratio of 6×10^6.

layer. For MHP thin-film FETs, this means that a fourth step is necessary, in which the MHP layer is manually patterned (Figure 1a) to prevent crosstalk between the multiple devices on the substrate, leading to most of the MHP being scratched or wiped off the substrate. The necessary patterning in combination with the spin-off of most of the precursor solution make spin coating a wasteful method, with only a fraction of the deposited material being used in the final device.

Using the high performance MHP thin-film FETs based on $Cs(Sn_{0.9}Pb_{0.1})I_3$ reported by Liu et al. as starting point, [16] we optimized and adapted the device architecture to the environment and processes of our laboratory. This led to a bottom gate, bottom contact architecture, which is shown in Figure 1b. We used a Cu gate and 100 nm Al_2O_3 as dielectric material, which was deposited using atomic layer deposition (ALD). The Au source/drain contacts were thermally evaporated, and the transistor channels were 150 µm long and 1 mm wide. This architecture was used for all devices presented in this work. Liu

et al. showed that the on/off ratio and the field effect mobility can be increased by substituting 10 % of the Sn with Pb and adding SnF_2 as a hole suppressor, which also significantly reduced hysteresis. This led to the final MHP composition $Cs(Sn_{0.9}Pb_{0.1})I_3$ + 10 mol% SnF_2 M, which was spin coated on top of the Au contacts.

Figure 1c shows optical microscope images of such a spin coated MHP thin-film FET. The MHP covers the entire channel and Au source/drain contacts homogeneously, with a few larger crystallites on top of the Au contacts especially. The MHP layer is around 30 nm thick. The output characteristics are shown in Figure 1d. The curve shows a linear relation between the drain source voltage (V_{DS}) and the drain source current (I_{DS}) for small V_{DS} and starts to saturate at a V_{DS} around −10 V. Furthermore, the device shows almost no hysteresis in the output curves. Figure 1e shows the transfer characteristics of the same device. The transfer shows a clear saturation, as well as a clear turn off around 25 V. The device shows a calculated charge carrier mobility of 2.2 $cm^2 V^{-1} s^{-1}$, an on/off ratio of 6×10^6 and a V_{th} of 0 V.

While the fabricated FETs do not achieve the same carrier mobility values as reported by Liu et al., most likely due to the necessary changes in device architecture, the results form the basis for comparison with the IJP MHP thin-film FETs.

2.2 | Full-Substrate Printed FETs

To transfer the deposition of the MHP layer from spin coating to IJP, we started with the full-substrate printing approach, trying to replicate the spin coating process as closely as possible with IJP. The process of full-substrate printing is shown in Figure 2a. Like spin coating, the entire substrate is covered with the MHP ink during printing, followed by annealing the wet film on a hotplate. Afterward, like spin-coated films, the annealed MHP film must be manually patterned analogously to the spin coating process, to ensure no crosstalk between the multiple devices on a single substrate. Therefore, this process does not yet take full advantage of the DOD IJP process, but enables the fabrication of comparable IJP MHP thin-film FETs, while avoiding challenges that occur with printing smaller areas, which will be shown in the next section.

In comparison to spin coating, IJP leads to a thicker wet film after deposition and therefore also to thicker MHP layers. To compensate this effect the concentration of the precursor solution was lowered from 0.4 to 0.1 M resulting in a 50 nm thick MHP layer. Figure 2b,c, respectively, show the output and transfer characteristics of an IJP MHP thin-film FET using the full-substrate printing approach. The output curves start to saturate around −15 V between source and drain and show no hysteresis. This also applies to the transfer curve, which is completely free of hysteresis and shows an on/off ratio of 2×10^6. In comparison to the spin coated benchmark device, the turn off voltage increases to $V_{off} = 55$ V at the gate as well as the threshold voltage, which increases to $V_{th} = 2$ V at the gate and the charge carrier mobility decreases to 1.6 $cm^2 V^{-1} s^{-1}$.

These impressive results mark the first step in transferring the deposition method of the perovskite layer in MHP thin-film FETs from spin coating to IJP, proving that it is possible to print MHP films for their use in thin-film FETs. However, to truly take advantage of the IJP process, in a next step we decrease the size of the printed features and directly print the necessary pattern.

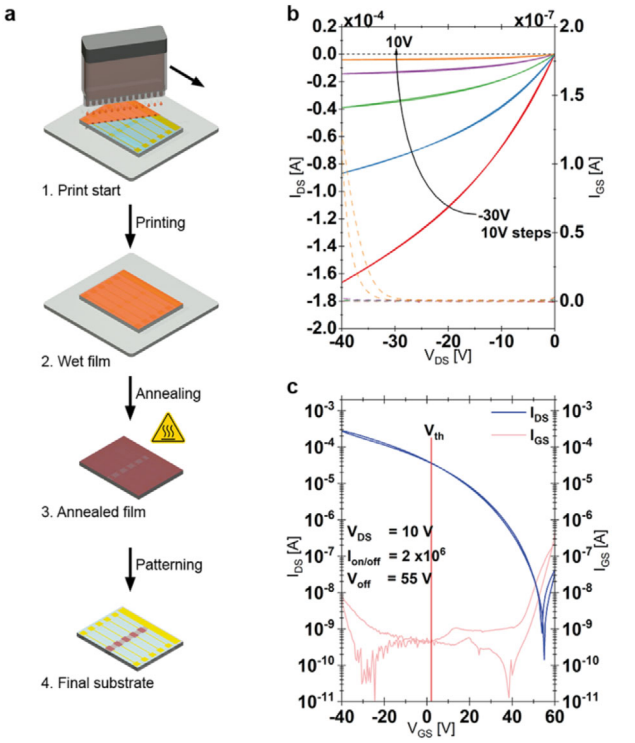

FIGURE 2 | (a) Full-substrate printing process of MHP thin-film FETs including the necessary patterning step. (b) Output and (c) transfer characteristics of a IJP MHP thin-film FET with almost no hysteresis and an on/off ratio of 2×10^6.

2.3 | In-Channel Printed FETs

After proving that IJP is a viable deposition method for perovskite layers in MHP thin-film FETs, the next step in completing the transfer from spin coating to IJP is to exclusively deposit the MHP inside the transistor channel.

The process of this in-channel approach is shown in Figure 3a. This process takes advantage of the fact that IJP is a DOD technique, resulting in a distinct printed pattern. In the case of the specific substrates used for our thin-film FETs we deposited the ink directly in the channel of the five devices that are on each substrate and not on the area around and between the devices. Afterward the wet pattern was then annealed on a hotplate, leading to the final perovskite film. This process works without the patterning of the MHP layer after annealing, making it faster, simpler and integrable into more complex processes. Furthermore, it is more sustainable than spin coating and full-substrate printing because it produces almost no waste. However, the printing of smaller areas comes with new challenges, mostly due to the more complex drying process at drop edges, which can lead to so-called coffee rings, making it harder to obtain even and controlled crystallization.

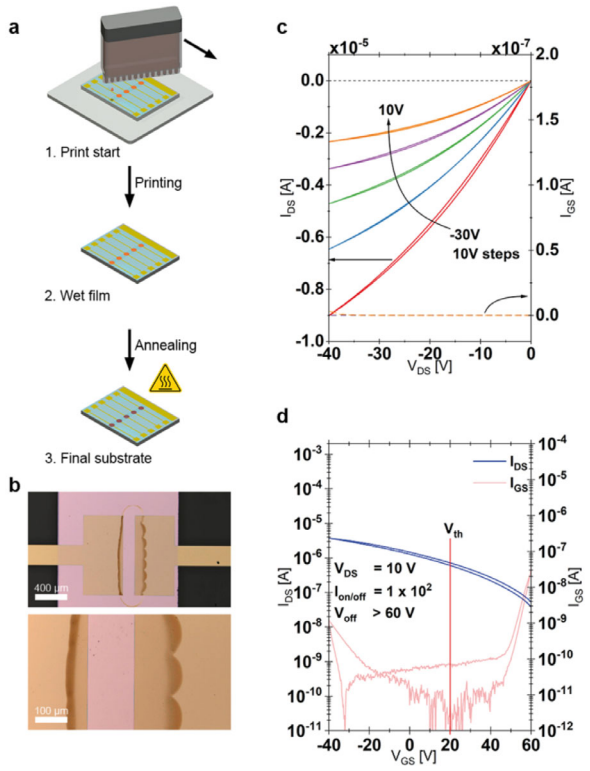

FIGURE 3 | (a) In-channel printing process of MHP thin-film FETs showing direct patterning as advantage of IJP. (b) Optical microscopy image of the printed MHP layer covering only the transistor channel. (c) Output and (d) transfer characteristics of an in-channel printed MHP thin-film FET.

Figure 3b shows optical microscopy images of an MHP thin-film FET that was fabricated using in-channel printing. For the MHP layer, a line of eight drops of ink was deposited on top of the 1 mm × 150 µm transistor channel leading to a complete coverage of the transistor channel. The MHP layer inside the channel is homogeneous and around 15 nm thick, only the edges of the line clearly show an agglomeration of crystallized material at the edge of the film caused by flow dynamics during the drying process ("coffee ring effect") [28]. This coffee ring has a negative effect on the device performance, which can be seen in both the output characteristics in Figure 3c and the transfer characteristics in Figure 3d. While there is still a clear dependence of the drain/source current I_{DS} in the output curves, the curves start to saturate only weakly around −20 V at the gate. This behavior can be explained by the presence of parasitic ohmic currents, which add to I_{DS} but are not controlled by the gate potential. These parasitic ohmic currents might occur due to the presence of the multiple micrometer thick coffee ring, because the gate field impacts only the gate-near region of the channel sufficiently. In combination with the fact that the devices are always-on devices, i.e. conductive even if no gate voltage is applied, this means that the gate-far regions of the coffee ring act as a conductive connection between the source and drain contacts. The effect of these parasitic ohmic currents is also visible in the transfer characteristics (Figure 3d) leading to an increase in the turn off voltage to $V_{off} > 60$ V and the threshold voltage $V_{th} = 20$ V as well as a decrease in the on/off ratio to 1×10^2 and the charge carrier mobility to 0.02 $cm^2\ V^{-1}\ s^{-1}$.

Nevertheless, besides the ohmic currents, the devices still show transistor characteristics. Figure S1 shows statistical data for all three deposition methods, demonstrating the reproducibility of the results. For each method, six devices were compared with respect to the performance parameters: on/off ratio, charge-carrier mobility, and threshold voltage. The statistical data show a reasonable spread in performance values, which can be attributed to the inherently complex crystallization behavior of perovskites, leading to slight variations in the final layer quality.

2.4 | Impact and Mitigation of Coffee Ring Effect

As discussed above, the device performance decreased in comparison to the full-substrate printing, due to the coffee ring effect. To investigate the influence of the coffee ring effect on the characteristics of thin-film FETs, we increased the printed area. This should decrease the impact of the coffee ring, because the ratio between the border and the inner part of the printed area is shifted toward the inner part.

We therefore printed a device in which the MHP layer covers not only the channel but also the source/drain contacts, resulting in an almost round MHP film, which is around 2 mm in diameter. Figure 4a shows an optical microscopy image of such a device. Even though the printed area is significantly larger than the area in Figure 3b, there is still a strong coffee ring visible. The coffee ring effect is reflected in the output and transfer characteristics, which are shown in Figure 4b,c, respectively. Both in the output and in the transfer characteristics the presence of ohmic currents can be seen, leading to the same effects as seen for the in-channel printed devices in Figure 3c,d. The output curves do not saturate, and the device does not turn off up to 60 V at the gate, again resulting in an on/off ratio of only 1×10^2 between −20 and 60 V at the gate.

To verify the coffee ring as the reason for the decrease in performance in comparison to the full-substrate printed devices, we manually separated the coffee ring of the just discussed device. An optical microscopy image of the resulting MHP layer with the separated coffee ring is shown in Figure 4d. The areas over and under the transistor channel, where the coffee ring was separated, are clearly visible, showing that the source and drain contacts are no longer connected by the coffee ring, while the MHP layer inside the transistor channel stays unchanged.

The output and transfer characteristics of the MHP thin-film FET with separated coffee ring are shown in Figure 4e,f. As expected, the output curves start to saturate stronger and earlier in comparison to the device with the coffee ring still intact. The overall flowing source/drain current decreases due to the absence of ohmic currents of the connecting coffee ring. The same trend can be seen in the transfer characteristics, where again the overall source/drain current decreases, while the device can now be turned off at 66 V at the gate, resulting in an increase in the on/off ratio of over three orders of magnitudes to 3×10^5. The coffee ring effect is therefore the main reason for the decrease in performance of small area printed MHP thin-film FETs in comparison to full-substrate printed devices. Mitigating it through increased print area and manual separation of the coffee ring recovers devices performance significantly.

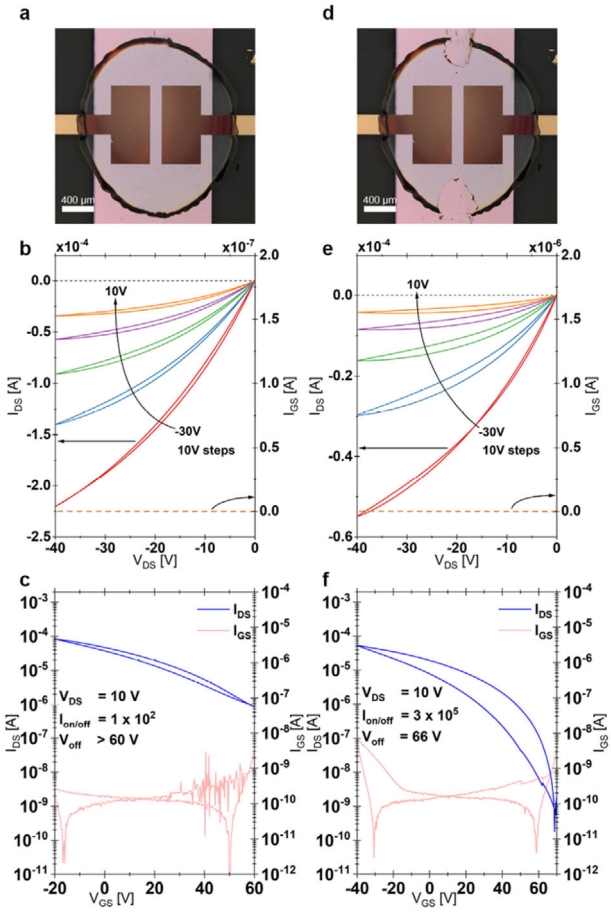

FIGURE 4 | (a) Optical microscopy image of a MHP thin-film FET with connected coffee ring and the respective output (b) and transfer (c) characteristics. (d) Optical microscopy image of the same MHP thin-film FET with manually separated coffee ring and the respective output (e) and transfer (f) characteristics.

These are promising results toward fully printed integrated circuits incorporating MHP thin-film FETs, showing the general capability of IJP for fabricating working small area MHP thin-film FETs. However, to overcome the limitations discussed in this study, further practical strategies will need to be developed, such as overcoming the coffee ring effect through ink formulation and engineering as well as refinement of the printing and drying parameters. Furthermore, substrate surface engineering through self-assembled monolayers, which promote uniform formation of MHP layers, as well as tuning the device architecture by integrating passivation layers, improving device reproducibility and stability are promising methods to improve the performance of future IJP MHP thin-film FETs [13, 29, 30].

3 | Conclusion

In this study, we explored the capabilities and limitations of IJP as an alternative deposition method for MHP layers in thin-film FETs, comparing its performance to the conventional spin coating technique and pushing the boundaries of this new approach for MHP thin-film fabrication of FETs. Our initial spin-coated benchmark devices showed a charge carrier mobility of 2.2 cm^2 V^{-1} s^{-1}, a high on/off ratio of 6×10^6 and a V_{th} of 0 V. Two distinct methods were then used to transition to IJP: full-substrate printing and in-channel printing. Full-substrate printing successfully replicated the spin-coated device characteristics to a significant extent, yielding clear transistor behavior and an on/off ratio of 2×10^6, with a slight decrease in mobility to 1.6 cm^2 V^{-1} s^{-1} and a V_{th} of 2 V. This confirmed the viability of IJP as an alternative to spin coating, while already reducing material waste albeit without taking advantage of the patterning capabilities of IJP. To fully leverage the additive fabrication nature of IJP, the in-channel printing approach was implemented, demonstrating, that direct patterning of MHP layers in thin-film FETs is possible and drastically reduces material waste. Devices fabricated with this approach initially suffered from a performance loss in comparison to the full-substrate approach with a reduced mobility of 0.02 cm^2 V^{-1} s^{-1} and on/off ratio of 1×10^2. However subsequent experiments confirmed that the main reason for the decrease in performance is related to the coffee ring effect. Mitigating this effect through increased print area and manual separation of the coffee ring recovered device performance significantly, improving the on/off ratio by over three orders of magnitude. This study advances fully printed MHP-based integrated circuits by identifying key challenges and outlining paths for optimization. Future improvements will focus on ink and process refinement, surface engineering, and device architecture tuning to enhance performance and stability.

4 | Experimental Section/Methods

4.1 | Substrate Preparation

All substrates were cleaned in an ultrasonic bath subsequentially in isopropanol and acetone for 5 min and dried with a N_2 gun, followed by oxygen plasma cleaning (Diener Femto, 0.35 mbar, 500 W, 1000 sccm) for 5 mins. Using a shadow mask, the gate electrode consisting of Cr (5 nm, 0.05 nm/s, 4×10^{-6} mbar) as an adhesion layer and Cu (50 nm, 0.12 nm/s, 4×10^{-6} mbar) was evaporated via physical vapour deposition. Afterward, the substrates were plasma treated as before, transferred inside a N_2 filled glovebox and 100 nm Al_2O_3 was deposited by atomic layer deposition (Arradiance GEMStar). The substrates were plasma treated again and immersed overnight in a 5 mM solution of octadecylphosphonic acid (ODPA) in isopropanol, leading to formation of a self-assembled monolayer (SAM). After the SAM treatment, the substrates were rinsed with isopropanol, dried using a N_2 gun and transferred to a cleanroom (ISO 7), where the photoresist AZ nLOF 2035 (MicroChemicals) was deposited via spin coating (60 s, 3000 rpm, 500 rpm/s) to yield an approx. 3 µm thick film. Subsequently, the substrate were soft baked at 110°C for 60 s, exposed in a lithograph (µPG 101 Heidelberg, 15 W, 75%, 1 × 1) and post exposure baked at 110°C for 60 s. Then the substrates were developed for 90 s in AZ 826 MIF developer and plasma-treated again. The source-drain electrodes were formed by evaporating Cr (5 nm, 0.05 nm/s, 4×10^{-6} mbar) followed by Au (50 nm, 0.12 nm/s, 4×10^{-6} mbar). Afterward, the substrates were immersed in TechniStrip overnight for the lift off of the photoresist. The substrates were then plasma-treated again and transferred to a N_2-filled glovebox for deposition of the MHP layer. The final

devices had a channel length of 150 µm and a channel width of 1 mm.

4.2 | Solution Preparation

All steps performed during the solution preparation were carried out in a N_2-filled glovebox. All precursors were supplied by TCI. The $CsSn_{0.9}Pb_{0.1}I_3$ (0.4 M for spin coating, 0.1 M for IJP) precursor solution with a ratio of CsI:(SnI_2 + PbI_2) of 1.25:1 was prepared by dissolving the respective amount of CsI, SnI_2 and PbI_2 powder in DMF and shaking it at 60°C overnight. The SnF_2 solution (6 mg/mL) was prepared by dissolving SnF_2 powder in DMF and shaking it at 60°C overnight. Right before deposition, the SnF_2 solution was added to the $CsSn_{0.9}Pb_{0.1}I_3$ solution to obtain a solution with 10 mol% of SnF_2 with respect to (SnI_2 + PbI_2).

4.3 | Thin-Film Deposition

All devices were plasma-treated in an oxygen plasma (Diener Femto, 0.35 mbar, 500 W, 1000 sccm) and then transferred to a N_2-filled glovebox, right before processing. All spin-coated MHP layers were statically spin-coated (Süss Micro Tec, 150 s, 4000 rpm, 500 rpm/) by placing 60 µL of the precursor solution in the middle of the substrate. Afterward the substrates were annealed (5 min, 120°C). After annealing, the MHP layer beside and in between the five devices on the same substrate was scratched away using a Q-tip soaked in DMF on the still hot substrate. All printed devices were processed using a PixDro LP50 with Spectra SE-128 (Fujifilm) print heads. Then the devices were dried using gas flow-assisted vacuum drying (GAVD) [25]. Therefore the devices were placed in an aluminum chamber, which was evacuated for 10 s, reaching a base pressure of ~1 mbar. After evacuation, a valve was opened to allow and control the nitrogen flow over the substrate for 30 s. During the 30 s under nitrogen flow, the crystallization of the perovskite layer started. Afterward, the devices were transferred to a hot plate for full crystallization and annealing (5 min, 120°C). For the "full-substrate" printed substrates, the MHP layer beside and in between the five devices on the same substrate was scratched away using a Q-tip soaked in DMF on the still hot substrate after annealing.

4.4 | Device Characterization

All the output and transfer characteristics were measured with a Keithley 4200A-SCS parameter analyzer using the Clarius measurement software. The devices were contacted using an Ossila low density OFET test board connected to the parameter analyzer via a BNC connection. All measurements were carried out under the same conditions in ambient light to ensure comparability. The charge carrier mobility values for the FETs are calculated from the linear regime of the transfer characteristics. All microscopy images were taken with an Olympus confocal laser microscope (LEXT OLS4100) after the devices were measured and transferred from the N_2-filled glovebox to ambient air. Layer thickness was measured with a profilometer from Bruker (Dektak XT).

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Conflicts of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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Supporting Information

Additional supporting information can be found online in the Supporting Information section.

Supporting File: aelm70291-sup-0001-SuppMat.docx.