

Amorphous/crystalline silicon heterojunction solar cells with black silicon texture

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Excellent passivation of black silicon surfaces by thin amorphous silicon layers deposited with plasma enhanced chemical vapor deposition is demonstrated. Minority charge carrier lifetimes of 1.3 milliseconds, enabling an implied open circuit voltage of 714 mV, were achieved. The influence of amorphous silicon parasitic epitaxial growth and thickness, as well as of the texture depth is investigated. Furthermore quantum efficiency gains for wavelengths above 600 nm, as compared to random textured solar cells, are demonstrated in 17.2% efficient amorphous-crystalline silicon-heterojunction solar cells with black silicon texture.

I. INTRODUCTION

The random, high aspect ratio nanoscale surface texture, which is commonly called black silicon, has excellent anti-reflection and light scattering properties and its successful application on the front surface of solar cells has recently been shown¹⁻³. The major challenge is the passivation of recombination active defects on the nanostructured and enlarged black silicon surface⁴. Previous works aiming at the application of black silicon in solar cells employ dielectric passivation layers¹⁻³. AlO_x layers deposited with atomic layer deposition for passivation of nanotextured silicon fabricated with reactive ion etching resulted in a few milliseconds minority carrier lifetime⁵ and 18.7% solar cell efficiency³. However, the alternative route of both passivation and contacting of black silicon with hydrogenated amorphous silicon (a-Si:H) has not been investigated. Hydrogenated amorphous silicon (a-Si:H) can provide excellent passivation of crystalline silicon surfaces and enables the electrical contacting of silicon wafers at the same time. Furthermore the use of amorphous-crystalline silicon heterojunctions (a-Si:H/c-Si-SHJ) is a proven concept for high-efficiency silicon solar cells⁶. The combination of the excellent optical properties of black silicon with the high quality surface passivation of amorphous silicon becomes even more interesting as the a-Si:H/c-Si-technology moves towards thinner wafers in order to realize even higher open circuit voltages⁷.

II. EXPERIMENTAL

For the present study 280 μm thick (100) and (111) oriented 1-5 Ωcm phosphorus-doped float zone silicon wafers were used as substrate material. Black silicon was fabricated by metal-assisted etching (MAE) of (100) Si

wafers, as described in earlier work⁸. Only one sample surface was textured, while the other remained planar. The samples were stripped of their native oxide in HF (5%). One nanometer of gold was evaporated, leading to isolated gold islands on the samples. Texture etching was carried out in a 1:5:20 solution of HF (50%), H₂O₂ (30%) and water at room temperature. For gold removal the samples were treated for 2, or 4 min in iodine and potassium iodine solution (I₂:KI:H₂O = 1:4:40 weight ratio). A SC1 cleaning step was applied to remove nanoporous material⁹.

Prior to a-Si:H deposition the wafers were cleaned following the RCA procedure and dipped in diluted hydrofluoric acid (3 min, 1%) to strip off the surface oxide. A-Si:H layers were deposited using plasma-enhanced chemical vapor deposition (PECVD). Intrinsic and doped layers were deposited at 0.5 mbar, with 60 MHz excitation and a silane flow of 10 sccm. 2 sccm diborane, or phosphine were added to deposit n- and p-type a-Si:H respectively. A hydrogen flow of 5 sccm was applied during the deposition of intrinsic layers. Doped layers were deposited using a plasma power density of 18 mW/cm² and 56 mW/cm² were applied for intrinsic layer deposition. The substrate temperature was 130°C for p-doped and intrinsic layers, but 195°C for n-doped layers. The distance between electrode and substrate was 19 mm for intrinsic layers and 23 mm for doped layer deposition. Intrinsic layers ((i)a-Si:H) were exposed to a hydrogen plasma treatment to decrease the interface defect density¹⁰. Process parameters of the hydrogen plasma treatments were 0.4 mbar, 130°C substrate temperature, a hydrogen flow of 20 sccm, 15 mm electrode to substrate distance and a power density of 112 mW/cm².

Indium tin oxide (ITO) layers were deposited using reactive radio frequency sputtering from an ITO target and 0.1% oxygen in the process gas flow. Metal contacts were fabricated by thermal evaporation. Front grids consist of a 10 nm titanium adhesion layer and 1.5 μm of silver. 10 nm of titanium and 500 nm of silver constitute the full area back contacts. A photoconductance decay setup (Sinton Consulting WCT-100) was used for mi-

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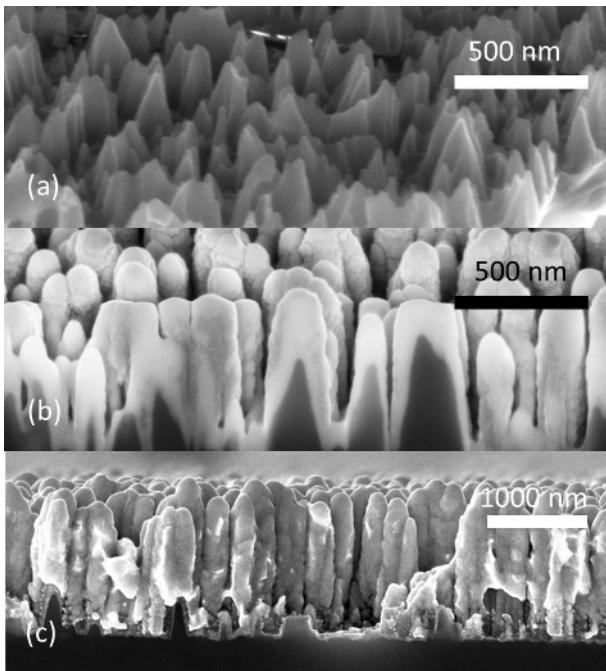


FIG. 1. SEM pictures of black silicon fabricated by 70 s of MAE and covered with 15 nm a-Si:H (a), 15 nm a-Si:H and 95 nm ITO (b) and a-Si:H, ITO and nominally 1.5 μm Ag (c).

minority carrier lifetime measurements¹¹, a Hitachi S4100 with cold field emitter for Scanning electron microscopy (SEM) and a Perkin Elmer Lambda 19 spectrometer for optical measurements.

The effective reflectivity of the textured surfaces is calculated from 300 to 1200 nm using the ASTM G173 spectrum as irradiation.

III. RESULTS AND DISCUSSION

The black silicon surfaces exhibit an effective reflectivity of 3.3 to 4.7% in the range from 300 to 1200 nm, compared to about 7% for an alkaline texture. The effective reflectivity value does not change after deposition of a-Si:H layers with deposition times of up to 60 s yielding a thickness of 30 nm, since the amorphous silicon follows the contour of the nanotexture and has a refractive index similar to the one of crystalline silicon. Depositing ITO layers with a nominal thickness of 90 to 95 nm decreases the effective reflectivity to about 2.3 to 2.5%. Because the refractive index of ITO lies between the refractive indexes of silicon and air. Therefore the grading of the reflective index between air and the silicon wafer¹² already brought about by the black Si texture is further flattened out. SEM images of black silicon covered with a-Si:H (Fig. 1a) and with a-Si:H and ITO (Fig. 1b) are displayed. The roughly conformal coverage of the nanotexture with ITO is visible. The average texture height is in the range of 500 nm.

One major challenge for passivation of a-Si:H/c-Si-HJs is

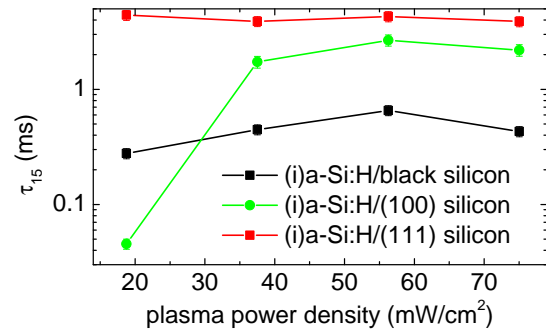


FIG. 2. Dependence of the minority charge carrier lifetime τ_{15} at an injection level of 10^{15}cm^{-3} on the plasma power density during intrinsic layer deposition. A post-deposition annealing step (200°C, 20 min) was applied to these samples. Values for planar (100), planar (111) and black silicon surfaces (70 s MAE) are displayed. Lines are guides to the eye.

the preparation of passivation layers with high structural quality without parasitic epitaxial growth¹³. This is a severe restriction on (100)-surfaces, but far less problematic on (111)¹³. As metal assisted etching (MAE) progresses preferentially along the $\langle 100 \rangle$ direction¹⁴ this could restrict the achievable passivation quality on black silicon. One parameter that allows to change from amorphous to epitaxial silicon growth is the plasma power density¹⁵. By increasing the power density the deposition rate increases, reducing the structural quality of a-Si:H and thereby preventing epitaxial growth. Therefore the a-Si:H passivation quality on black silicon is explored as a function of the plasma power density. Furthermore the epitaxial growth has to be identified. It is known that thermal annealing at 200 to 300°C improves passivation of atomically sharp a-Si:H/c-Si-interfaces¹⁶, but leads to a degradation of the minority carrier lifetime for interfaces with partial epitaxial growth¹⁷. Therefore a post deposition annealing step at 200°C for 20 min was applied to discriminate between epitaxy free samples and those with partial epitaxy.

Minority carrier lifetime values for planar and nanotextured samples passivated with intrinsic a-Si:H deposited at varying plasma power densities are shown in Fig. 2. Intrinsic amorphous silicon deposition times of 30 s, corresponding to film thicknesses of about 15 nm, are chosen for planar (111) and (100) wafers, while deposition times of 60 s are chosen for black silicon to account for the higher aspect ratio. The planar back side of the black silicon samples is passivated with 4 nm intrinsic a-Si:H deposited at 56 mW/cm².

A change in the plasma power density from 36 to 18 mW/cm² results in a drop of the minority carrier lifetime on (100) Si by more than one order of magnitude. A similar, but less pronounced, lifetime decrease is visible for black silicon samples. In contrast, (111) samples do not experience any drop in lifetime in the depicted parameter range. Therefore it can be assumed that the

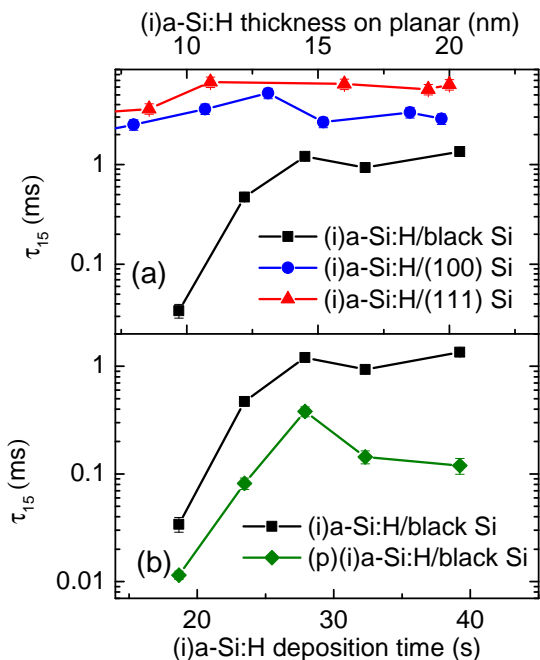


FIG. 3. Minority charge carrier lifetimes τ_{15} at an injection level of 10^{15} cm^{-3} (a) in dependence of the intrinsic passivation layer deposition time and thickness on planar wafers for (100), (111) and black silicon wafers. (b) black silicon with passivation layers and after the deposition of p-doped layers on the black silicon side and n-doped layers on the untextured side. Etch time for the black silicon samples was 70 s. Lines are guides to the eye.

black silicon surface possesses a similar tendency towards epitaxial growth as (100) silicon surfaces.

In a second parameter variation the amorphous silicon passivation layer thickness was varied on planar and on black-textured samples. The dependence of minority carrier lifetime on the passivation layer deposition time and thickness is shown in Fig. 3a. Due to the high aspect ratio a thicker amorphous silicon layer is needed for effective passivation of black silicon. While the passivation of planar wafers with amorphous silicon already reaches saturation at an amorphous silicon thickness of 10 nm, the black silicon samples are most likely not even fully covered at this thickness and the passivation saturates only at about 15 nm film thickness. Furthermore the maximum lifetime is smaller for the black silicon surfaces, possibly due to the enlarged surface area and thus the higher total number of defects. The difference between (100) and (111) surfaces can be explained as being due to the higher density of dangling bonds on (100) surfaces compared to the (111) surface. The overall higher minority carrier lifetime of the black silicon samples in this second experiment are attributed to more thorough removal of gold residuals by prolonged etching (4 minutes).

The thickness value for which the minority charge carrier lifetime saturates can be used to deduce the surface

increase due to the nanotexture as compared to a planar surface. Fujiwara and Kondo¹⁸ found that a-Si:H on a planar wafer changes from interface layer structural properties to bulk layer properties at a thickness of about 4 nm. They also observed a saturation of open circuit voltage and thus lifetime at this thickness. The same saturation can be found for the nanotextured surfaces at about 15 nm. This determines the surface increase due to the nanotexture to about a factor of 3.5 to 4 compared to a planar surface and is in agreement with experiments using SEM and atomic force microscopy⁹.

The best lifetime value achieved during these experiments is 1.3 ms, enabling 714 mV implied open circuit voltage. This high minority carrier lifetime has been achieved on fully nanotextured surfaces with an effective reflectivity of about 3% using a passivation layer with 15 nm nominal thickness.

The application of black silicon in a-Si:H/c-Si solar cells necessitates to form a p/n-junction and apply a back-surface field using doped a-Si:H layers. In Fig. 3b minority carrier lifetimes of black silicon samples with passivation layers and after deposition of n-type layers on the untextured side and p-type layers on the textured side are depicted. As can be seen in Fig. 3b, the lifetime values of all samples deteriorate drastically, corresponding to an implied V_{OC} decrease from 715 to 655 mV for the sample with a 15 nm thick passivation layer. This effect is known from planar and alkaline textured a-Si:H/c-Si structures and is typically explained by Fermi level shift induced defect generation¹⁹. Still the degradation is stronger for the passivation layers on black silicon, as the planar reference only degrades from 730 mV to 725 mV implied V_{OC} . Possible reasons are a different physical structure of the intrinsic amorphous silicon due to the growth on the black silicon surface, lateral inhomogeneous a-Si:H thicknesses, or gold residuals from the metal assisted etching process. Solar cells were fabricated using these samples and the IV characteristics and internal quantum efficiency (IQE) were measured. A strong decrease of the blue response for the black silicon solar cell as compared to a KOH textured reference is visible in Fig. 4.

One possible reason for decreased blue response is enhanced carrier recombination in a nanoporous region at the black etched surface²⁰. A SC1 cleaning step is able to remove these nanoporous regions⁹ and was applied during the experiments presented here. Therefore parasitic absorption in nanoporous silicon can be excluded.

Another possible reason is parasitic absorption in amorphous silicon layers. To investigate whether this is the reason for the IQE decrease, the internal quantum efficiency of two solar cells with 70 s metal assisted etching time, but different intrinsic a-Si:H deposition times are shown in Fig. 4. Although there is a slight decrease of the IQE with increased a-Si:H thickness, it is obvious that this cannot be the reason for the strong blue deficiency of the nanotextured solar cells.

A third reason could be enhanced Auger recombination¹, or parasitic absorption in the nanotex-

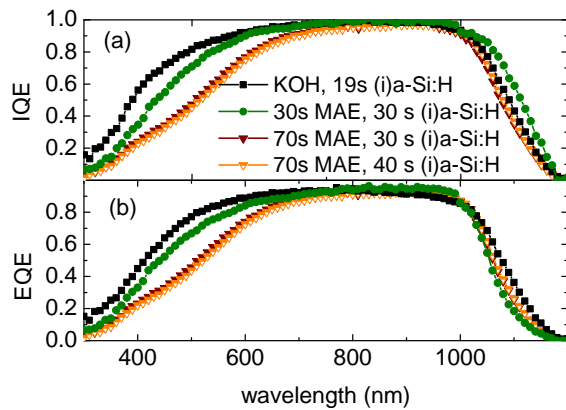


FIG. 4. (a) Internal quantum efficiency (IQE) of solar cells with KOH texture and 19s intrinsic a-Si:H deposition time for the front side, compared to the IQE of solar cells with two black silicon texture times (70s and 30s) and two (i)a-Si:H deposition times (30s, or 40s). P-type a-Si:H deposition time was 50s for the black silicon texture and 15s for the KOH texture. (b) External quantum efficiency (EQE) of the same devices.

ture. Therefore a solar cell with a 30s long black silicon etch was fabricated, leading to a more shallow texture and an effective reflectivity of about 10%. The IQE of this solar cell is also shown in Fig. 4a. For this solar cell only a slight decrease of the blue response is visible. Therefore the IQE decrease appears to be due to parasitic absorption, or enhanced recombination in the nanotexture. A possible reason for this parasitic absorption is that the p-type emitter surrounding the nanotexture enforces a majority carrier type inversion in the small structures. This could prevent the collection of minority carriers from this region.

The solar cell with 30s MAE time has an efficiency of 17.2%, a fill factor of 77.4%, a short circuit current of 34.2mA and an open circuit voltage of 649mV. Thereby displaying better output parameters than the solar cell constructed on the 70s texture, which has only 31.7mA short circuit current, due to its lower blue response, an open circuit voltage of 604mV and a fill factor of 72.7%. Leading to an efficiency of 13.9%. Compared to a solar cell with random pyramid texture, a short circuit current of 36.2mA and an efficiency of 20.2% the 30s black silicon solar cell has an improved quantum efficiency for all wavelengths higher than 700nm. Still the Fermi-level shift induced degradation of the passivation layers decreases the open circuit voltage well below the 707mV, which were achieved applying the same deposition parameters on a planar (100) wafer.

IV. CONCLUSION

It was shown that it is possible to passivate black silicon surfaces with a-Si:H. The passivation layer thick-

ness has to be increased by at least a factor of three compared to planar surfaces to reach high quality passivation, which concurs with earlier measurements of the planar-to-textured surface ratio⁹. Furthermore investigations indicate, that black silicon surfaces exhibit a similar tendency towards epitaxial growth as (100) surfaces. Black silicon surfaces show great promise for the application in a-Si:H/c-Si solar cells since implied open circuit voltages of about 714mV have been reached for initial passivation layers, as well as excellent optical properties with reflectivities below 5%. Amorphous-crystalline silicon heterojunction solar cells with black silicon front surface exhibiting a promising efficiency of 17.2% and gain in quantum efficiency compared to random pyramid textures for wavelengths above 600nm have been fabricated.

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