

Tailoring nano-textures for optimized light in-coupling in liquid phase crystallized silicon thin-film solar cells

Grit Köppel^{*}, David Eisenhauer^{**}, Bernd Rech, and Christiane Becker

Helmholtz-Zentrum Berlin für Materialien und Energie, Kekuléstraße 5, 12489 Berlin, Germany

Received ZZZ, revised ZZZ, accepted ZZZ

Published online ZZZ (Dates will be provided by the publisher.)

Keywords silicon thin-film solar cell, nanoimprint lithography, light management, sub-wavelength grating.

* Corresponding author: e-mail grit.koeppel@helmholtz-berlin.de, Phone: +49 30 8062 13644, Fax: +49 30 8062 41333

Thin-film solar cells based on liquid phase crystallized silicon (LPC Si) with 8-20 μm thick absorber layers demand for advanced light management to achieve high photocurrent densities (j_{sc}). Open-circuit voltages >600 mV underline the high material quality of LPC Si thin-films being grown and crystallized on nano-textured glass superstrates. We present hexagonal sinusoidal superstrate textures which provide enhanced light in-coupling for LPC Si thin-film solar cells. 500 nm-pitched sinusoidal nano-textures are found to outperform larger pitched superstrate textures with respect to reducing reflection losses at the buried glass-silicon interface. In the wavelength range of interest reflection of incident light is minimized to values close to 4%, which is the reflection at the sun-facing air-glass interface. The

superior optical properties of 500 nm-pitched sinusoidal gratings have been predicted by optical simulations. Here, the successful experimental realization is presented. Further, the electronic material quality of sinusoidally textured devices is analysed on basis of a comparison of maximum achieved open-circuit voltages (V_{oc}) on different texture types. Changing the interlayer deposition method from PVD RF magnetron sputtering to a PECVD process enabled a V_{oc} of 630 mV on sinusoidal textured substrates. Thus, we are able to unify high optical and electronic properties of silicon absorber layers on sinusoidal textured glass substrates. These results constitute a crucial step towards fully exploiting the optical potential of liquid phase crystallized silicon thin-film solar cells.

Copyright line will be provided by the publisher

1 Introduction Recent advances in Liquid Phase Crystallization (LPC) of thin-film silicon enabled reaching an electronic material quality comparable to silicon wafer material [1]. A major limitation in current liquid phase crystallized (LPC) silicon thin-film record solar cells on glass are optical losses at different interfaces [2]. Light management is a common challenge in thin-film solar cells, which is often addressed by texturing of various interfaces [3-7]. In current LPC solar cells optical losses are reduced by adding an anti-reflective layer to the sun-facing air-glass interface and by applying wet-etched pyramidal textures as well as reflectors at the rear side of the device enabling cell efficiencies of up to 13.2% [8]. However, in order to exploit the full optical potential of LPC silicon thin-film solar cells, an anti-reflective texture at the buried glass-silicon interface is required. This texture should not only increase light in-coupling into the active layer but at

also be able to maintain the electronic material quality of the absorber layer being grown and crystallized on this texture. This challenge is faced in former publications [9-11]. Hexagonal sinusoidal nano-textures with a period of 750 nm have demonstrated to be one promising approach to overcome this trade-off enabling a maximum achievable short-circuit current density of 37.0 mA/cm² if combined with additional measures for light trapping at the absorber layer rear side [12]. However, numerical studies predicted that absorption enhancement can be further increased if decreasing the texture period down to 500 nm – 600 nm [13,14].

In this paper, we provide experimental evidence of the superior optical properties of 500 nm-pitched sinusoidally textured samples compared to a larger 750 nm-pitched sample as well as a state-of-the-art planar reference. In a second step an analysis of the electronic material quality is

provided by comparing the maximum achieved open circuit-voltages on differently textured glass superstrates. This demonstrates that the 500 nm sinusoidal texture constitutes a promising candidate for optimized light incoupling in LPC silicon thin-film solar cells.

2 Sample Preparation All devices were prepared in superstrate configuration on 5 cm x 5 cm x 1.1 mm large Corning Eagle XG® glasses being coated with a 250nm thick SiO_x diffusion barrier. For texturing the superstrates were coated with an approximately 600nm thick high-temperature stable UV-curable SiO_x sol-gel. 500 nm and 750 nm-pitched hexagonal sinusoidal nano-textures fabricated by interference lithography [15] were transferred onto the superstrates by nanoimprint lithography.

For optical characterization textured and planar superstrates were coated either with a 10 nm SiO_x-layer or a 70 nm SiN_x / 10 nm SiO_x layer stack by PVD RF magnetron sputtering. The latter is commonly featured in state-of-the-art planar LPC Si thin-film solar cell devices [1]. Subsequently, nano-crystalline silicon absorber layers of the desired thickness were deposited by electron beam evaporation at 600°C heater temperature. Absorber layers being intended for optical analysis only were deposited by electron beam evaporation at 300°C and subsequently solid phase crystallized (SPC) by thermal annealing for 20h at 600°C [16]. This is a quick and facile process and optical material properties do not differ from LPC silicon in the analyzed wavelength range being well below 900nm [17]. For electronic characterization the absorber layers were n-doped with a doping concentration of approximately $5 \cdot 10^{16} \text{ cm}^{-3}$ and crystallized by being scanned with a line shaped 808nm laser beam with a scanning velocity of 3mm/s. This liquid phase crystallization process allows for high quality silicon absorber layer material with grains that are up to a few centimetres in length and up to a few millimeters in width [1]. If a textured superstrate and a 250 nm SiO_x capping layer are used during crystallization, double-sided textured absorber layers are obtained [9] as it is also the case for the SPC process. After removal of the capping layer by etching for 5min in a 5% HF-solution, a contacting scheme as described in Ref. [1] is applied, there denoted by test structure.

The superstrate texture morphology was analyzed using a Park Systems XE-70 AFM equipped with high aspect-ratio tips. Optical characterization was conducted by means of a Perkin Elmer LAMBDA 1050 spectrometer within an integrating sphere with a diameter of 15cm. For electronic characterization the Suns-Voc unit of a WCT-100 photoconductance lifetime tool by Sinton Instruments was used.

Schematics of the respective sample stacks for optical and electronic characterization as well as atomic force microscope (AFM) scans of 500 nm and 750 nm-pitched glass superstrates are depicted in figure 1.

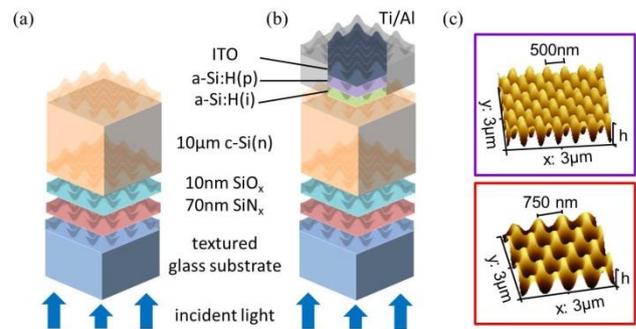


Figure 1 Schematic of the device structure (a) for optical characterization, (b) for electronic analysis and (c) AFM images sinusoidally textured glass substrates with a fixed aspect ratio (h/P) of about 0.25 and varied periods (P) of 500 nm (purple) and 750 nm (red).

3 Results and Discussions

3.1 Absorption Properties The influence of the sinusoidal texture period on the optical properties of 10 µm thick silicon absorber layers are studied by comparing samples with a fixed aspect ratio of about 0.25 and varied periods (P) of 500 nm ("Sine P500") and 750 nm ("Sine P750") as well as a state-of-the-art planar reference. We restrict our analysis to a wavelength range $<650 \text{ nm}$ because this is the wavelength range of interest with respect to light in-coupling at the glass-silicon interface. Light trapping at the silicon absorber layer rear side can be optimized individually [12] and is, thus, not part of this study specifically addressing the light in-coupling properties of differently sized sinusoidal glass superstrate textures.

For both periods samples with and without additional anti-reflexive SiN_x layer are analysed. The samples without SiN_x layer demonstrate the sole influence of the texture's period on the optical properties without being superimposed by the influence of an additional anti-reflective coating. The corresponding absorptance spectra are plotted in figure 2a. The samples with SiN_x / SiO_x interlayer stack represent absorber layers intended for implementation in LPC solar cell devices. The optical properties of these devices are analysed in figure 2b.

In figure 2a both textured samples, the 500 nm-pitched Sine (purple) and the 750 nm-pitched Sine (red) are found to outperform their respective planar references with optimized interlayer stack (black). The light in-coupling ability into the silicon absorber layer of the 500 nm-pitched device exceeds the larger 750 nm-pitched texture. Despite absolute differences becoming smaller, these findings are preserved if adding an anti-reflective SiN_x-layer to the sample stacks (Fig. 2b). The combination of a 500 nm-pitched sinusoidal superstrate texture with a SiN_x-layer enables absorption close to 96% (dotted line) over a broad wavelength range.

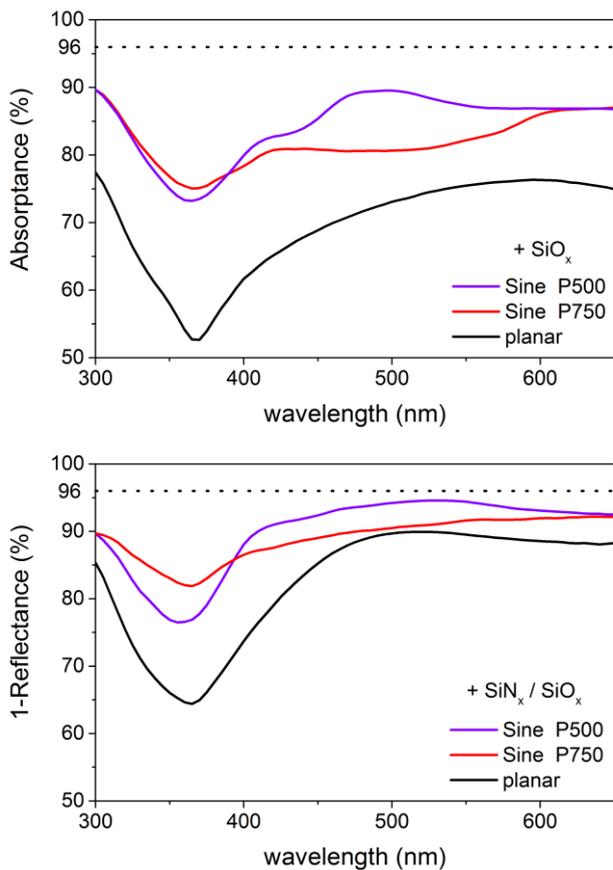


Figure 2 Absorbance of 500 nm-pitched (purple) and 750 nm-pitched (red) sinusoidally textured silicon absorber layers as well as a planar reference (black) with a thickness of $10\mu\text{m}$ (a) with a 10 nm SiO_x layer and (b) with a 70 nm SiN_x / 10 nm SiO_x interlayer stack providing additional anti-reflective properties.

This 96% benchmark serves as an upper achievable boundary since 4% of the incident light are reflected at the air-glass interface when light first encounters the device. Only for wavelengths longer than about 640nm the larger 750 nm-pitched sinusoidal sample starts to outperform the smaller 500 nm-pitched sample. In this part of the spectrum absorption enhancement originating from the front interface texture is superimposed by light being partially scattered back into the device at the rear side texture. This rear side is only reached by light with wavelengths longer than the penetration depth. Hence, it is expected from geometrical optics that light scattering at the rear side is more pronounced for the larger period with higher and broader structure features.

In order to allow for a more quantitative evaluation, mean absorbance values were calculated averaging over a wavelength range from 350nm to 600nm. Adding a SiN_x -layer increases mean absorbance A in case of the planar device (black) by $\Delta A = + 13.9\%$ (absolute) to 82.6%, in case of the 750 nm pitched device by $\Delta A = + 8.1\%$ to 88.8%, and in case of the 500 nm-pitched device by

$\Delta A = + 6.0\%$ to 90.5%. Since sinusoidal textured glass substrates already provide anti-reflective properties, the effect of adding a SiN_x coating to textured devices is less pronounced than in the planar case. Indeed, the 500 nm-pitched sinusoidal texture without additional anti-reflective coating exceeds the planar reference featuring a SiN_x layer by $\Delta A = +1.9\%$ (absolute). Thus, texturing the absorber layer enhances absorption more effectively than using a state-of-the-art anti-reflective SiN_x coating in a planar device. Comparing the samples featuring an anti-reflective SiN_x coating the 750 nm-pitched sample increases mean absorbance by 6.2% (absolute), while the 500 nm-pitched sample raises mean absorbance by 7.9% (absolute) compared to the planar reference. Therefore, here we successfully demonstrated the experimental realization of superior anti-reflective properties of the 500 nm-pitched hexagonal sinusoidally textured sample as it was predicted by simulations of Lockau et al. [13] and Jäger et al. [14].

3.2 Material Quality The suitability of a nano-texture for implementation at the buried glass-silicon interface is not only determined by its light in-coupling property but it also has to allow for a high electronic material quality. One convenient measure to quantify a sample's electronic material quality is measuring the open-circuit voltage (V_{oc}). Table 1 not only lists the V_{oc} achieved on 500 nm-pitched sinusoidal nano-textures but also puts these results into context by reviewing open-circuit voltages achieved on different texture types so far. As not being deposited in the same batch, distinct differences arise between the samples listed related to processing (e.g. different interlayer and silicon absorber layer thicknesses). For processing details please refer to the specific reference given along with the V_{oc} . Thus, these values are not directly comparable but rather serve as guideline for future cell design developments. Moreover, in order to further enhance the material quality of the silicon absorber layer, a recently developed PEVCD process for interlayer deposition in planar LPC silicon thin-film solar cells [8] was adapted for textured superstrates as a change from a PVD to a PECVD interlayer deposition process promises enhanced coverage of the texture flanks. The respective results are listed in table 1.

The steep texture flanks of the $2\mu\text{m}$ square lattice texture with an aspect ratio of 0.5 were found to give rise to dislocation lines proceeding throughout the entire absorber layer. This distortion of silicon material quality caused the external quantum efficiency to drop [9]. A similarly disturbed electronic material quality was found if using steep pillar textured superstrates with feature sizes about half of the square lattice. For the pillar texture a high amount of defects being present in the silicon absorber layer were revealed by Secco defect etching [10]. Smooth statistically etched random and MST textured superstrates provided good electronic properties reflected by high open-circuit voltages. However, only little optical

Table 1 Maximum achieved open-circuit voltages (V_{oc}) on differently textured LPC silicon thin-film solar cells. As further details, the texture period, the interlayer deposition method, and the silicon absorber layer thickness are listed. In addition to the record open-circuit voltages the respective references are given.

Texture	Period, Interlayer deposition, Si thickness	Max. V_{oc}	Ref.
Square Lattice	2 μm , PVD, 10 μm	539mV	[9]
Random	- , PVD, 10 μm	616mV	[9]
MST	- , PVD, 15 μm	634mV	[18]
Pillar	750 nm, PVD, 10 μm	492mV	[10]
SMART	750 nm, PVD, 8 μm	649mV	[11]
Sine	750 nm, PVD, 10 μm	618mV	[10]
Sine	500 nm, PVD, 10 μm	601mV	(this paper)
Sine	500 nm, PECVD, 14 μm	630mV	(this paper)

and thus, cell performance improvement was found compared to the planar reference devices [9,18].

Among the textures reviewed so far highest light in-coupling improvement was found for the pillar texture. Therefore, two texture types were developed based on the pillar texture. First, a sinusoidal texture maintaining the pitch and height of the pillar texture but smoothing out the texture flanks [10]. Second, a smooth anti-reflective three-dimensional texture that fills the voids of the pillar texture with TiO_x as index matching material [11]. The 750 nm-pitched sinusoidal texture was able to improve the electronic material quality with respect to the steep pillar texture to a level being comparable to the planar reference device. However, this texture still suffered from current losses in the intermedium wavelength range [10]. On the contrary, the almost flat textured glass superstrate-silicon interface of the SMART texture directly enabled a high silicon material quality with an open-circuit voltage of 649 mV exceeding its planar reference [11].

The 500 nm-pitched sinusoidal texture newly introduced in this study was only able to achieve similarly high open-circuit voltages when changing the interlayer deposition method from RF magnetron sputtering to a PECVD method allowing for better coverage of the texture flanks. This new interlayer deposition method enhancing the silicon absorber layer quality was recently developed for planar LPC silicon devices, there contributing to a cell efficiency of 13.2% [8]. Using this superior interlayer stack compared to the PVD sputtered interlayers used before enabled an open-circuit voltage of 630 mV on a sinusoidally textured glass superstrate. Thus, the 500 nm-pitched texture not only features the best optical properties of all textures analysed so far but also offers a high silicon material quality at the same time.

4 Conclusion We successfully implemented 500 nm-pitched sinusoidal nano-textures at the buried glass-silicon interface of 10 μm -15 μm thick silicon thin-film devices. The 500 nm sinusoidal texture outperformed larger pitched superstrate textures with respect to enhancing light in-coupling at this interface reducing the reflection loss close to 4% over a broad wavelength range. In the analysed cell design this 4% reflection loss is unavoidable as no anti-reflective measures are taken at the sun-facing air-glass interface and therefore, marks an upper achievable boundary for textures at the glass-silicon interface. Moreover, with this study we provided the experimental realization of an optimized light in-coupling texture as it was predicted by simulations. If an advanced interlayer stack deposited by PECVD is used, these superior optical properties are accompanied by a high electronic material quality of the silicon absorber layer. The latter is reflected by a maximum achieved open-circuit voltage of 630 mV achieved on a 14 μm thick LPC silicon absorber layer being grown and crystallized on a 500 nm-pitched glass superstrate. Therefore, this texture has proven to be a promising candidate for future LPC silicon thin-film solar cell designs.

Acknowledgements The authors gratefully acknowledge the support of M. Krüger, C. Klimm and H. Rhein, HZB. The German Federal Ministry of Education and Research (BMBF) is acknowledged for funding the research activities of the Young Investigator Group Nanostructured Silicon for Photonic and Photovoltaic Implementations at Helmholtz-Center Berlin in the program NanoMatFutur (no.03X5520).

References

- [1] J. Haschke, D. Amkreutz, L. Korte, F. Ruske, and B. Rech, *Sol. Energy Mater. Sol. Cells* **128**, 190-197 (2014).
- [2] T. Frijnts, S. Kühnapfel, S. Ring, O. Gabriel, S. Calnan, J. Haschke, B. Stannowski, B. Rech, and R. Schlatmann, *Sol. Energy Mater. Sol. Cells* **143**, 457-466 (2015).
- [3] A. Polman, M. Knight, E.C. Garnett, B. Ehrler, and W.C. Sinke, *Science* **352**, aad4424 (2016).
- [4] M.Z. Pakhuruddin, J. Huang, J. Dore, and S. Varlamov, *IEEE J. Photovoltaics* **6**, 159-165 (2016).
- [5] K.X. Wang, Z. Yu, V. Liu, Y. Cui, and S. Fan, *Nano Lett.* **12**, 1616-1619 (2012).
- [6] M. Peters, M. Rüdiger, H. Hauser, M. Hermle, and B. Bläsi, *Prog. Photovoltaics Res. Appl.* **20**, 862-873 (2012).
- [7] M. Boccard, C. Battaglia, S. Hänni, K. Söderström, J. Escarré, S. Nicolay, F. Meillaud, M. Despeisse, and C. Ballif, *Nano Lett.* **12**, 1344 (2012).
- [8] P. Sonntag, N. Preissler, M. Bokalič, M. Trahms, J. Haschke, R. Schlatmann, M. Topič, B. Rech, and D. Amkreutz, *Sci. Rep.* **7**, 873 (2017).
- [9] V. Preidel, D. Amkreutz, J. Haschke, M. Wollgarten, B. Rech, and C. Becker, *J. Appl. Phys.* **117**, 225306 (2015).
- [10] G. Köppel, B. Rech, and C. Becker, *Nanoscale* **8**, 8722 (2016).
- [11] D. Eisenhauer, G. Köppel, K. Jäger, D. Chen, O. Shargaieva, P. Sonntag, D. Amkreutz, B. Rech, and C. Becker, *Sci. Rep.* **7**, 2658 (2017).

- 1 [12] G. Köppel, D. Eisenhauer, B. Rech, and C. Becker, *Opt.*
2 *Express* **25**, A467-A472 (2017).
- 3 [13] D. Lockau, M. Hammerschmidt, J. Haschke, M. Blome, F.
4 Ruske, F. Schmidt, and B. Rech, *Proc. SPIE* 9140, 914006
5 (2014).
- 6 [14] K. Jäger, G. Köppel, C. Barth, M. Hammerschmidt, S.
7 Herrmann, S. Burger, F. Schmidt, and C. Becker, in *Proc.*
8 *SPIE*, edited by R.B. Wehrspohn, A. Gombert, and A.N.
9 Sprafke (2016), p. 989808.
- 10 [15] A.J. Wolf, H. Hauser, V. Kübler, C. Walk, O. Höhn, and B.
11 Bläsi, *Microelectron. Eng.* **98**, 293-296 (2012).
- 12 [16] C. Becker, D. Amkreutz, T. Sontheimer, V. Preidel, D.
13 Lockau, J. Haschke, L. Jogschies, C. Klimm, J.J. Merkel, P.
14 Plocica, S. Steffens, and B. Rech, *Sol. Energy Mater. Sol.*
15 *Cells* **119**, 112-123 (2013).
- 16 [17] D. Lockau, T. Sontheimer, C. Becker, E. Rudigier-Voigt, F.
17 Schmidt, and B. Rech, *Opt. Express* **21**, A42 (2013).
- 18 [18] G. Köppel, D. Amkreutz, P. Sonntag, G. Yang, R. Van
19 Swaaij, O. Isabella, M. Zeman, B. Rech, and C. Becker,
20 *IEEE J. Photovoltaics* **7**, 85-90 (2017).
- 21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57