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Stacking fault reduction during annealing in Cu-poor $CuInSe_2$ thin film solar cell absorbers analyzed by in-situ XRD and grain growth modeling

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ABSTRACT

Buried wurtzite structures composed by stacking faults of the {111} planes in zinc-blende and {112} planes in chalcopyrite structures can result in barriers for charge carrier transport. A precise understanding of stacking fault annihilation mechanisms is therefore crucial for the development of effective deposition processes. During co-evaporation of $Cu(In,Ga)Se_2$ – a photovoltaic absorber material showing record efficiencies of up to 22.9 % for thin film solar cells – a reduction of stacking faults occurs at the transition from a Cu-poor to a Cu-rich film composition, parallel to grain growth, which is suggesting that the two phenomena are coupled. Here, we show by *in-situ* synchrotron X-ray diffraction during annealing of Cu-poor $CuInSe_2$ thin films, that stacking faults can be strongly reduced through annealing, without passing through a Cu-rich film composition. We simulate the evolution of the XRD stacking fault signal with a simple numerical model of grain growth driven by stacking fault energy and grain boundary curvature. The results support the hypothesis that the stacking fault reduction can be explained by grain growth. The model is used to make predictions on annealing times and temperatures required for stacking fault reduction and could be adapted for polycrystalline thin films with similar morphology.

I. INTRODUCTION

Many semiconductor materials used in polycrystalline thin film solar cells and other functional thin film devices share the basic diamond structure as fundamental crystal feature. The {111} lattice planes in the diamond structure of Si and zinc-blende CdTe, ZnO, ZnS correspond to {112} lattice planes in kesterite-type $Cu_2ZnSnSe_4$ and Cu_2ZnSnS_4, and chalcopyrite-type $Cu(In,Ga)S_2$, $Cu(In,Ga)Se_2$ (CIGS) and $CuInSe_2$ (CIS). Stacking faults of these planes can easily form during film growth due to low stacking fault energies [1, 2, 3, 4, 5]. Moreover, stacking faults may cause barriers for majority charge carriers by forming buried wurtzite structures [6, 7]. More complex planar defects [8] and their terminating dislocations [9] likely have even stronger effects on the electronic properties of the material. In particular, for stacking faults bounded by a Frank-type dislocation loop it has been shown that they induce deep defect states which enhance non-radiative recombination [10]. In CIS, stacking faults (including twins) have been observed by transmission electron microscopy (TEM) [11, 12, 13], with higher densities found at lower growth temperatures [11]. Their presence appears to lower the mobility of charge carriers [14]. Therefore, for the synthesis of high-quality semiconductor films from these materials, it is important to understand and control the reduction of stacking faults. An XRD feature characteristic for planar defects of the 112 planes, such as stacking faults and twin boundaries – sometimes also referred to as twin stacking faults [15] - allows to observe their evolution *in-situ* during or after film growth.

Recent reports on CIGS absorbers with efficiencies of up to 22.9 % [16] - currently the highest confirmed efficiency within the field of polycrystalline thin-film solar cells – highlight the relevance of this compound semiconductor. A three-stage co-evaporation process, during which In-Ga-Se is deposited in a first step, followed by Cu-Se in a second stage and a final In-Ga-Se deposition, is commonly used for high-efficiency CIGS absorbers [17, 18]. It has been shown, that a high density of stacking faults may form in this process during the transformation from the hexagonal $(In,Ga)_2Se_3$ phase to the tetragonal $Cu(In,Ga)Se_2$ phase [15, 13]. However, the Cu-poor/Cu-rich transition during the Cu-Se deposition of the three-stage process leads to a nearly complete annihilation of stacking faults [13], even at low growth temperatures (450 °C and below) that are relevant for solar cells on flexible, light-weight polymer substrates [19, 20, 21, 22]. To achieve a simplification of the process and hence a cost-reduction of solar module fabrication, it is interesting to know whether the favorable effects of the Cu-poor/Cu-rich transition – including the reduction of stacking faults – could instead be achieved by annealing

while maintaining Cu-poor composition, and which temperatures and annealing times would be required.

In the present work, we investigate the annihilation of stacking faults in Cu-poor CIS thin films by synchrotron-based *in-situ* X-ray diffraction (XRD). *In-situ* XRD is uniquely suited to record the relative evolution of the stacking fault density, because in contrast to microscopy images the measurement is continuous and a much higher number of grains contribute to the signal. Our results reveal that the stacking fault signal in Cu-poor CIS samples can be strongly reduced through annealing at higher temperatures above 570 °C, without passing through a Cu-rich film composition.

While in principle stacking faults could annihilate via different mechanisms, stacking fault reduction during Cu-deposition in the three stage process has been shown experimentally to coincide with grain growth in CIS and CIGS [13, 14]. Parallel occurrence of stacking fault annihilation and grain growth has also been observed in SiC [23]. The preferential growth of grains with fewer stacking faults could explain the annihilation of stacking faults through grain growth [14, 23]. To study if the energy of the stacking faults would in principle be sufficient to drive such preferential grain growth, we apply a simple numerical model for grain growth driven by generic energy density and curvature differences [24] to the case of stacking fault energy in CIS to simulate the evolution of the XRD stacking fault feature during sample heating. The results show that already energy differences between grains caused by relatively small stacking fault concentrations are sufficient to explain the experimentally observed decrease of stacking faults by grain growth. We use the model to make predictions on the reduction of stacking faults which can be achieved through annealing at different temperatures.

II. METHODOLOGY: EXPERIMENT AND MODEL

A. *In-situ* monitoring of stacking fault decrease

We measure the decrease of stacking faults during the annealing of Cu-poor CIS thin films by either *in-situ* energy-dispersive X-ray diffraction (EDXRD) or *in-situ* angle-dispersive X-ray diffraction (ADXRD). *In-situ* EDXRD measurements are performed with polychromatic synchrotron radiation at the EDDI beamline at BESSY II [25]. Two energy-dispersive Ge detectors [26] record diffraction peaks from lattice planes nearly parallel to the surface (detector 1) and with a tilt angle of ~ 65° between the lattice planes and the sample surface (detector 2).

The experimental setup is described in detail in [27, 28]. The incident, exit and diffraction angles are the same as in [29]. The probed volume is given by the irradiated area of 1 mm · 2.2 mm and the film thickness of about 1 µm. Planar defects of the 112 planes, such as stacking faults and twins, which are considered here as a special case of stacking faults, lead to a characteristic broadening of the 112 diffraction peak with an additional maximum (Fig. 2(a)). This additional maximum is caused by the disturbance of the chalcopyrite symmetry (see [13] for details). To extract the intensity evolution of the feature attributed to stacking faults (Fig. 2(a)) a peak fit with a Pseudo-Voigt function is performed, while keeping the width and position constant. A background reduction is realized by subtracting the average of the intensity from the last minute of the measurement, where the stacking fault feature is not discernable anymore (Fig. 2(b)).

In-situ ADXRD measurements are performed by using a laboratory setup with a Cu X-ray tube and a detector array. A detailed description of the setup can be found elsewhere [30, 31]. Here, the intensity of the stacking fault feature is extracted by summing up the intensity of the measurement points in a range of 0.7° around the position of the stacking fault feature at each time step after background subtraction. The intensity of the stacking fault feature is normalized with a factor calculated from the first data points corresponding to 2 min during which the sample remained at constant temperature.

B. Sample preparation and annealing

Cu-poor CIS films are synthesized by successively depositing In-Se (at 330 °C substrate temperature) and Cu-Se (at 420 °C for samples A, B, C and 360°C for samples D and E) by co-evaporation in a physical vapor deposition (PVD) chamber onto Mo-coated soda-lime glass substrates. The temperatures of 330 °C and 420 °C for the first and second stage of the three-stage process are typically used for deposition of CIGS for high-efficiency solar cells on flexible polyimide foil [21, 22]. Cu deposition is stopped at a Cu-poor composition ([Cu] / [In] < 1). To study the influence of the composition on the decrease of the stacking faults, the [Cu]/[In] ratio as well as the concentration of Na – which is used as dopant in CIS and CIGS [32] – were varied. Both possibly affect the mobility of grain boundaries and the stacking fault density [14]. Na is deposited as a 12 nm thick NaF film prior to CIS deposition. To prevent Na diffusion from the glass, all glass substrates are coated with a SiN_xO_y film as diffusion barrier. The [Cu]/[In] and Na variations of the samples are summarized in Table I.

The annealing of the samples is performed inside PVD chambers tailor-made for *in-situ* EDXRD or ADXRD analysis. For sample A, the full CIS film deposition and annealing are performed in the *in-situ* EDXRD chamber. For samples B and C, after the In-Se deposition the samples are transferred to the *in-situ* EDXRD chamber, where Cu-Se is deposited and subsequently the annealing started under Se background pressure. The substrate temperature is first kept constant at the deposition temperature for $5\,\mathrm{min} - 10\,\mathrm{min}$ before ramping up with a constant heating rate. Samples D and E are transferred to the *in-situ* ADXRD chamber after complete CIS deposition, where the annealing is started at temperatures (350°C for sample D and 300°C for sample E) below the deposition temperature of 360°C. For the EDXRD setup the temperature T is measured with a thermocouple placed between the substrate and the substrate heater, with an estimated systematic uncertainty of $\Delta T \pm 25\,\mathrm{K}$ for absolute values. For the ADXRD setup the temperature is measured with a thermocouple in direct contact with the substrate. (See Supplemental Material S.4.5 for discussion of the temperature measurement). An overview of the samples and the annealing conditions is given in Table I. To test consistency with the grain growth model described in section II.C, the heating rates are varied for the samples with Na (see Table I).

Tab. I: Overview of the CIS samples including use of a NaF precursor layer, Cu content, heating rate and in-situ XRD method used during annealing. [Cu]/[In] as determined by X-ray fluorescence measurements.

In-situ synchrotron-based EDXRD			
Sample	NaF	[Cu]/[In]	Heating rate
A	Yes	0.61	3 K/min
B	No	0.84	3 K/min
C	No	0.65	3 K/min
In-situ laboratory ADXRD			
D	Yes	0.85	2 K/min
E	Yes	0.85	5 K/min

C. Model for grain growth driven by energy density differences

Annealing in the temperature range described in the previous section has been shown to lead to grain growth in CIGS [36]. When the three-stage process is interrupted before the transition to a Cu-rich composition, the grain size of the resulting Cu-poor CIS and CIGS thin films is usually smaller than the film thickness [13][14][33][34]. The grain structure of samples interrupted at Cu-poor compositions has been observed to be more equiaxed [13, 14, 18] (in contrast to CIGS samples from complete processes at standard temperatures, which often show columnar grains).

If in such a structure only the reduction of the grain boundary energy acts as driving force, normal grain growth occurs, which can be described by using the curvature of the average grain radius [35, 36]. This approach has been used in a previous model to numerically describe grain growth in CIS [36]. In reality, grain growth can be assumed to additionally involve other driving forces, such as strain [27], surface energy [39], dislocation [38] and point defect energy, energetically favored grain shapes, and also stacking fault energy. Defects within grains – such as dislocations, point defects and stacking faults – lead to an increased internal energy of such grains compared to grains with fewer defects. Hence the total internal energy decreases by the growth of defect-poor grains on the expense of defect-rich grains, which additionally leads to a reduction of the average defect density of the material, as illustrated by a phase field model in Fig. 1: If all grains have the same internal energy, only grain growth driven by grain boundary energy is active and large grains grow on the expense of small grains (Fig. 1(a)). In contrast, if the internal energy of the grains varies between grains, smaller defect-poor grains may grow on the expense of larger defect-rich grains, given the energy difference is sufficient (Fig. 1(b)) (details of the phase field modeling can be found in the Supplemental Material S.1).

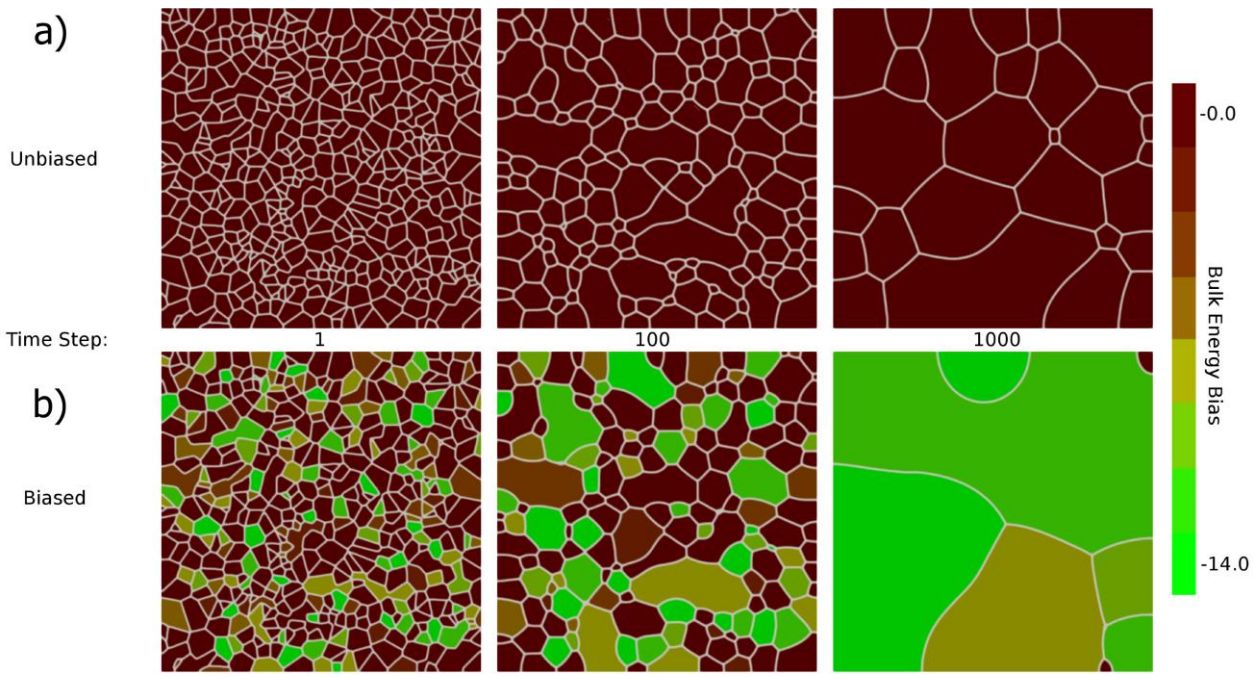

Fig. 1: (a) Phase field simulation of grain growth driven by grain boundary energy at three different time steps. (b) Phase field simulation of grain growth with an additional bulk energy bias at the same time steps.

Furthermore, the growth of grains with low defect density at the expense of grains with a high stacking fault density has been confirmed by in-situ scanning transmission electron microscopy (STEM) during the annealing of a Cu-poor CIS thin film with a Cu-Se capping layer [40]. Exemplary microscopy images are shown in Fig. S1 in the Supplemental Material.

It is important to note that without the contribution of the defect energy as driving force for grain growth, the grains will still grow due to grain boundary energy and potentially additional driving forces. But in this case, the average defect density of the material would not change. Only if the stacking fault energy and the variation of stacking fault density from grain to grain are sufficiently large, grain growth will lead to a reduction of the average stacking fault density.

We employ a simple statistical grain growth model to investigate if the energy of the stacking faults within the grains would be sufficient to drive preferential growth of grains with low stacking fault energy, and hence lead to the experimentally observed reduction of the average stacking fault density. While such a simplified grain growth model cannot give a completely accurate description of the complex microstructure evolution, it is used here to test the plausibility of grain growth as explanation for stacking fault reduction by simulating the evolution of the XRD stacking fault signal.

To consider the difference in stacking fault energy between grains as driving force, we use a model proposed by Deus et al. [24], which combines curvature driven grain growth with a driving force due to generic energy differences between grains. Hillert proposed a simple expression for the growth rate of an individual spherical grain, which is often used to describe curvature driven grain growth [37, 38]:

$$\frac{dr}{dt} = k_r \left(\frac{1}{r^*} - \frac{1}{r}\right) \quad (1)$$

where r is the radius of the grain and $k_r = \varphi M \gamma$. Here M is the grain boundary mobility, γ the specific free energy and φ a geometrical factor of the grain boundaries, all of which in this simple model are assumed to be equal for all grain boundaries. The critical radius r^* determines whether a grain with radius r will shrink ($r < r^*$) or grow ($r > r^*$). The condition of constant volume – no material is removed or added during grain growth – can be used to calculate r^* [24]. For three dimensional grains the result is:

$$r^* = \frac{<r^2>}{<r>} \quad (2)$$

Here, the angular brackets refer to the grain ensemble average. Equation (1) can be modified to account for an additional driving force caused by energy density differences [24]:

$$\frac{dr}{dt} = k_r \left(\frac{1}{r^*} - \frac{1}{r}\right) + k_E(E^* - E) \qquad (3)$$

with $k_E = \phi M$, where E is the energy density of the grain, ϕ is a shape factor and the grain boundary mobility M is assumed to be the same as in (1). (Note that the formula in [24] is given for the diameter of n-dimensional grains and therefore the values of the prefactors k_r and k_E are different.) The critical radius r^* and the critical energy E^*, which can be deduced respectively from the case of purely curvature and purely energy driven growth by applying the constant volume condition [24], are specific solutions of the combined case (see Supplemental Material S.3). In the three dimensional case E^* is given by

$$E^* = \frac{<r^2 E>}{<r^2>} \qquad (4)$$

A derivation of equation (2) and (4) can be found in the Supplemental Material S.3.

D. Application of grain growth model to $CuInSe_2$ polycrystalline thin films

Here, we apply the general approach for grain growth driven by energy density differences described in section II.C to the specific case of stacking fault energy densities in CIS thin films. A schematic visualization (based on TEM images of a Cu-poor CIGS thin film from a low-temperature process interrupted before reaching Cu-saturation [13]) of the model is given in Fig. 2(c): larger grains and grains with fewer stacking faults grow at the expense of smaller grains and grains with more stacking faults. The stacking fault density corresponds to an energy density. As a simplification we assume spherical grains and a homogenous stacking fault density within each grain. In our model twin regions are not considered as separate grains, because the straight twin boundaries do not contribute to curvature driven grain growth. Instead, the twin boundaries are treated as a special case of stacking faults, contributing to the stacking fault density of a grain. The grain growth model is three-dimensional. The thin films used for the experimental investigations have thicknesses of about 1 µm to 2 µm. Three-dimensional growth without surface effects can be assumed as long as the average grain sizes in the model is well below the film thickness, which is the case for Cu-poor CIS [13][14][33][34]. The grain size distribution in CIS thin films has been reported to be lognormal [41, 36]. For our simulations we use a normalized lognormal function with parameters μ_d and σ_d:

$$f(x) = \frac{e^{-(\ln(x)-\mu_d)^2/2\sigma_d{}^2}}{x\,\sigma_d\sqrt{2\pi}} \qquad (5)$$

The distribution of the diameter values d is obtained by substituting $x = d/g_d$, where

$$g_d = \frac{d^{exp}}{e^{\mu_d + \frac{\sigma_d{}^2}{2}}} \qquad (6)$$

is the ratio between the expectation value of the grain diameter d^{exp} and the expectation value of the dimensionless parameter $x^{exp} = e^{\mu_d + \frac{\sigma_d{}^2}{2}}$. No experimental information is available for the distribution of stacking fault density among the grains of polycrystalline CIS. Analogously to the grain size distribution, we arbitrarily describe the stacking fault density distribution by a lognormal function with an expectation value of the energy density E^{exp} and distribution parameters μ_E and σ_E. The grain boundary mobility is assumed to be thermally activated

$$M = M_0 e^{-Q/k_B T} \qquad (7)$$

Here, Q is the activation energy, k_B the Boltzmann constant, T the temperature and M_0 the temperature independent prefactor of the grain boundary mobility.

Altogether, the parameters of the model are the shape factors φ and ϕ, the free energy of the grain boundary γ, the activation energy Q, the initial expectation values of the grain size d^{exp} and energy density E^{exp}, the distribution parameters $\mu_d, \sigma_d, \mu_E, \sigma_E$, the grain boundary mobility factor M_0 and the temperature T. The initial values of the parameters are estimated based on literature values for CIS (where available; for the order of magnitude of the grain boundary mobility prefactor M_0 data on aluminum was used). See Appendix for details. The grain growth model described by Eq. (3) is implemented in a MATLAB script. Starting with N = 1 000 000 grains with a given grain size and stacking fault density distribution, we use Eq. (2),(3) and (4) to calculate the critical radius $r^*(t)$, the critical energy $E^*(t)$ and the new radius of each grain after the time step Δt. The simulated volume corresponds to about 0.5 % of the experimentally probed volume. According to XRD simulations, the intensity of the experimental stacking fault XRD feature is proportional to the average stacking fault density of the sample. In our model the stacking fault density of a grain is proportional to its energy density E. To track the evolution of the average energy density of the grain ensemble, we weight the energy density of each grain by its volume and sum over all grains. The resulting volume-weighted stacking fault energy density (E_{vw}) is used to compare the model with the experimental XRD data. To this end, the energy density E_{vw} curve is normalized to its initial value. An overview of the parameters with more details on the initial estimates and the simulation can be found in Supplemental Material S.4.

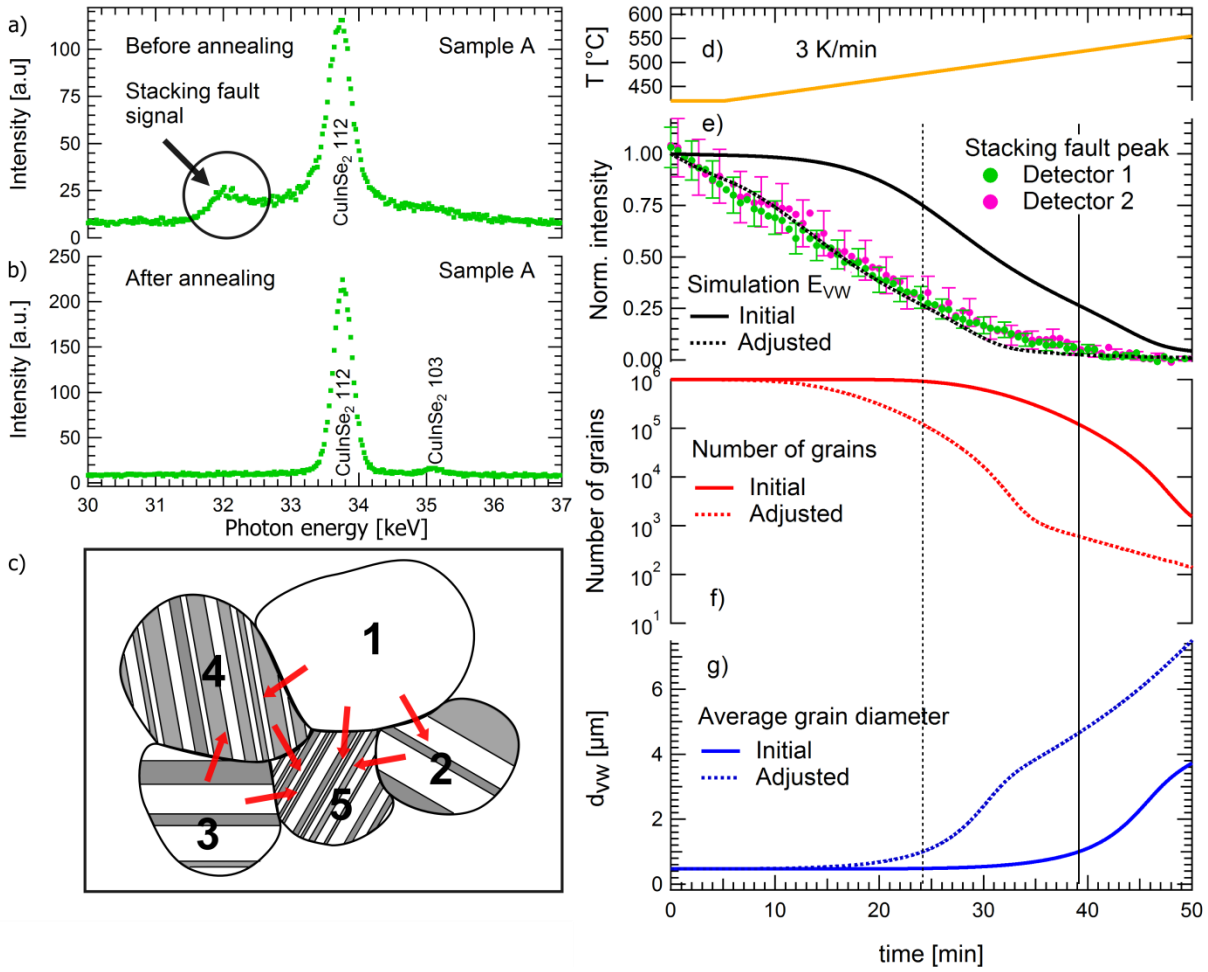

Fig. 2: (a) Diffractogram of a CIS sample with NaF after Cu deposition stop and before annealing. The stacking fault feature is marked by a black arrow. (b) Diffractogram of the same sample after annealing to 550°C. (c) Schematic of the grain growth model: a combination of grain size and stacking fault density is decisive for which grains grow (1,2,3) at the expense of others (4,5). (d) Substrate temperature profile during the experiment and simulation. (e) Time-resolved normalized intensity of the stacking fault feature as recorded by detector 1 and detector 2 with in-situ EDXRD for the same sample as in (a) and (b). The evolution of the volume weighted energy density E_{vw} is shown for a simulation with the initial parameter set (black solid line) and with adjusted activation energy Q (dashed black line). Evolution of the (f) number of grains and (g) volume-weighted average grain size d_{vw} for the initial parameter set (solid line) and with adjusted activation energy Q (dashed lines) during a simulation of 3000 s. The vertical black lines mark the moment when the simulated average grain diameter reaches the experimental film thickness of 1 µm for the initial parameter set (solid line) and with adjusted activation energy Q (dashed line). Error bars reflect standard deviation of counts. For better readability only every third error bar is represented.

III. RESULTS AND DISCUSSION

A. Experimental observation of stacking fault decrease

Fig. 2(d) describes the temperature profile to which sample A is subjected during the annealing procedure. The evolution of the stacking fault peak as recorded by detectors 1 and 2 during annealing is depicted in Fig. 2(e). The heating ramps are sufficiently low for the experiment to be considered as a series of isothermal conditions at the time scale of Δt =1s used for the simulations. It can be seen that the intensity of the stacking fault signal decreases as the substrate temperature increases. The signals from the two detectors are identical within the limits of the error bars, indicating that the decrease is not due to a texture change but to a real decrease of stacking fault density. It can be seen that heating the sample to 550°C is sufficient to reduce the stacking fault density below the sensitivity of the *in-situ* XRD measurement. The decrease of the stacking fault signal in Fig. 2(e) starts immediately, suggesting that stacking fault reduction through grain growth already occurs at the starting temperature of 420°C. To further investigate the temperature dependency of the stacking fault reduction, annealing experiments with two different heating rates and lower starting temperatures are performed. The samples D and E (like sample A with NaF precursor) are annealed with heating rates of 2 K/min (sample D) and 5 K/min (sample E). The experimental results shown in Fig. 3(d) and Fig. 3(f) confirm a thermal activation of the decrease of the stacking fault density, with an onset at about 420°C for the studied samples.

To analyze the effect of Na and Cu concentration on the decrease of stacking fault density during annealing we compare the *in-situ* EDXRD data of the CIS thin film with Na (sample A, Fig. 3(b)) with measurements from two samples without Na and different Cu content (samples B and C), which are depicted in Fig. 3(h) and Fig. 3(i). The difference between the evolution of the stacking fault signals of the two samples without Na - but varying Cu content - is smaller than the experimental uncertainty. Hence, we conclude that at Cu-poor conditions a different constant Cu concentration has no significant influence on the stacking fault reduction during annealing. During annealing of the sample A with NaF (Fig. 3(b)), the stacking fault signal decreases earlier and slightly steeper than for the samples B and C without NaF (Fig. 3(h),(i)).

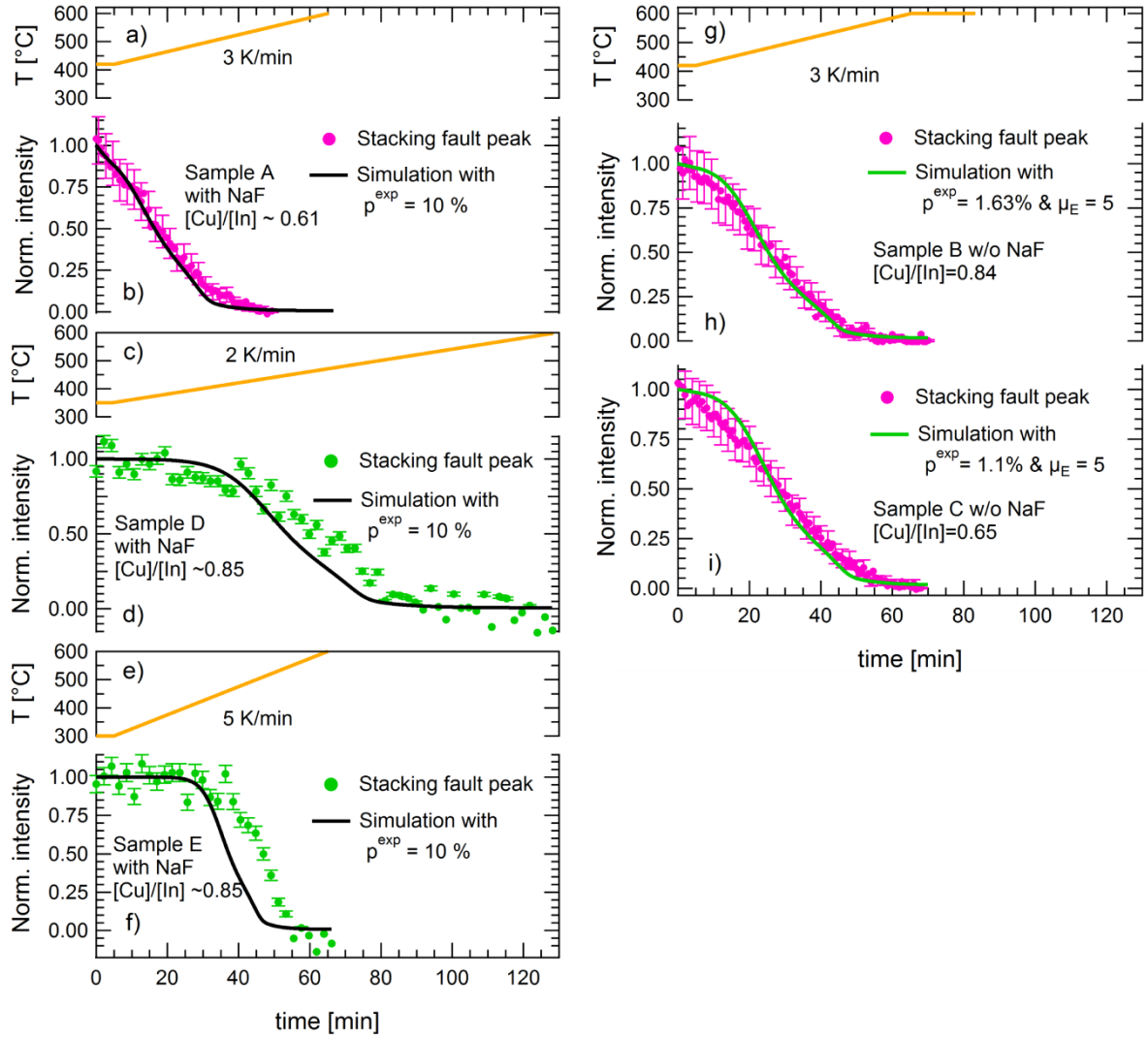

Fig. 3: In-situ EDXRD analysis and simulation of the stacking fault annihilation. (a),(c),(e),(g) Temperature gradient used for annealing and simulations below. (b),(d),(e),(f),(g),(i) Evolution of normalized measured XRD stacking fault signal (dots) and simulated energy density E_{vw} (solid lines) during annealing of CIS samples: Cu-poor samples with NaF precursor annealed with a heating rate of (b) 3 K/min (sample A, measured with EDXRD), (d) 2 K/min (sample D, ADXRD), and (f) 5 K/min (sample E, ADXRD). Negative data points at the end of the annealing are due to background subtraction (see section II.A.); Cu-poor samples without NaF precursor with (h) higher Cu content (sample B) and (i) a lower Cu content (sample C) annealed with a heating rate of 3 K/min, measured with EDXRD. For the simulations depicted as black lines in (b), (d) and (f) the initial parameter set (Tab.A.I) was used, with the activation energy modified to Q = 3.11 eV. For the simulations depicted in (h) and (i) p^{exp} was respectively set to 1.63% and 1.1% and μ_E increased from 2.5 to 5 (green lines).

Previous studies have shown that CIS [14] and CIGS [13] samples whose deposition was interrupted at a Cu-poor composition without further annealing exhibit grain sizes around 0.5 µm. After the transition to a Cu-rich composition the grains have grown to more than 1 µm [13, 14].

A SEM image of one of the annealed Cu-poor CIS thin films shows that grain sizes of about 1 µm can also be achieved after annealing, reaching the limit of the film thickness (Fig. 4(a)), while a Cu-poor CIS thin film prepared in the in-situ PVD chamber at 430°C without annealing shows smaller grains (Fig. 4(b)).

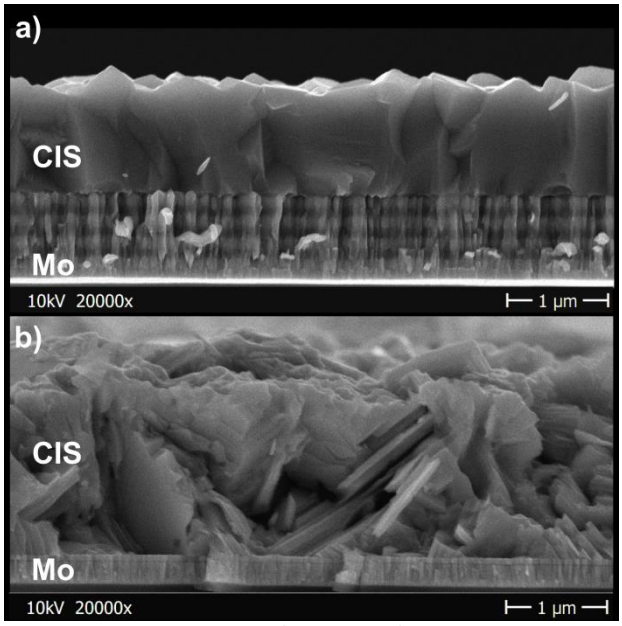

Fig. 4: SEM images of a) one of the annealed Cu-poor CIS thin films (sample B) and b) a Cu-poor CIS thin film without annealing.

B. Comparison of experimental data and simulation

A grain growth simulation with the initial parameter estimate from Table A.I and the temperature gradient of the annealing of sample A (Fig. 2(d)) results in the calculated evolution of number of grains depicted in Fig. 2(f) and the volume weighted average grain size (d_{vw}) shown in Fig. 2(g). It can be seen that the number of grains decreases from 1 000 000 to 1550 and the average grain size d_{vw} increases from 0.47 µm to 3.72 µm after 3000 s. The evolution of the simulated energy density E_{vw} is depicted in Fig. 2(e) (solid black line) together with the decrease of the intensity of the XRD stacking fault feature, as recorded by detector 1 and 2 with *in-situ* EDXRD during the annealing of sample A (dots). The vertical black line marks the point in time beyond which the simulated grain size exceeds the limit of the film thickness of 1 µm and the grain growth would no longer be predominantly three-dimensional, as assumed in the model. See Supplemental Material S.4.9 for a comparison of the simulation results for three- and two-dimensional grain growth.

While there is a clear offset between the experimental data and the simulated solid black line in Fig. 2(e), the simulation shows that with the initial parameter set based on literature data (Tab. A.I), the grain growth driving force induced by the distribution of stacking fault energy can qualitatively reproduce the experimentally observed reduction of the stacking fault density. The deviation is not surprising, considering the facts that (i) the parameters from the literature are - at least partially - only rough estimates, as described in the Appendix; (ii) the measured temperature has an uncertainty of estimated $\Delta T = \pm 25$ K; (iii) the grain growth model employed here simplifies the reality, e.g. by neglecting additional possible driving forces and limitations and by assuming spherical shape of the grains.

Nevertheless, the decrease of the simulated energy density shows that the assumed stacking fault energy would be sufficient to contribute as driving force to grain growth, and hence sufficient to lead to the observed decrease of the stacking fault density by preferential grain growth of defect poor grains. Even if the stacking fault energy from literature was reduced by a factor of 10, its magnitude would still be large enough to support preferential growth and the decrease of the simulated energy density would be only slightly shifted to higher temperatures by about 35 K (see Supplemental Material S.5).

Also variations of the initial grain size d^{exp} and geometrical factor ϕ within plausible limits only lead to small shifts in the temperature range of the decrease and induce almost no change of the curve shape. In contrast, variations of the prefactor (M_0) of the grain boundary mobility or its activation energy (Q) have a stronger influence on the temperature range of the decrease (see Supplemental Material S.6 with Fig. S6). For example, reducing the activation energy Q from 3.3 eV of the initial estimate to 3.11 eV leads to an evolution of the simulated energy density E_{vw} that coincides with the experimental data (dashed line in Fig. 2(e), solid black line in Fig. 3(b)).

Other parameters, such as the grain size and stacking fault distribution parameters μ_d, σ_d, μ_E, σ_E, mainly affect the slope of the simulated curve. A change of the free energy of the grain boundary γ over a range of two magnitudes (equivalent to a variation of the shape factor φ) has no significant effect on the E_{vw} curve, pointing to the effect of the stacking fault energy being much stronger than the one of the grain boundary energy with the given initial parameter set. See Supplemental Materials S.6 for details of all parameter variations.

We simulate the grain growth for the different annealing rates used in the measurements that are depicted in Fig. 3(d) and 3(f) with the same parameters (initial parameter set from Tab. A.I with adapted activation energy $Q = 3.11$ eV) as for the previously discussed sample A in Fig. 3(b). The resulting decrease of energy density E_{vw} is depicted as black line in Fig. 3(d) and Fig. 3(f). The simulated E_{vw} curves match the shape of the decrease of the stacking fault feature well, but are slightly shifted towards an earlier decline. This shift could be either due to small differences in sample properties like grain size and stacking fault distribution or caused by a temperature offset of the ADXRD experiments compared to the setup used for the synchrotron EDXRD experiments.

The annealing of samples with (Fig. 3(b)) and without NaF (Fig. 3(h),(i)) at identical heating rates shows that the stacking faults signal decreases earlier and slightly steeper in the sample with NaF than for the samples without NaF. Considering that Na segregates at grain boundaries [42, 43], where a precipitate can be expected to reduce grain boundary mobility [44], and previous results showing Na to impede stacking fault annihilation at the Cu-poor/Cu-rich transition of the three-stage process [14], this finding could be regarded as counter-intuitive. While a comparison with only one sample with Na is not sufficient to reliably determine the influence of Na, there are several possible explanations for the observed effect. It is possible that the NaF precursor layer – or the deposition in a different PVD chamber (see section II.B) – may affect the microstructure of the In_2Se_3 layer from the first stage of the three -stage co-evaporation in a way that subsequently leads to a faster grain growth during annealing, e.g. by leading to a finer grain structure or favoring the formation of grain boundaries with higher mobility. Also, a recent study [45] demonstrated an enhanced atomic diffusion within Cu-poor CIS grains due to Na presence, which could lead to additional stacking fault annihilation within grains during annealing, independent of grain growth. However, in polycrystalline CIS with grain boundaries, Na presence is known to reduce Cu diffusion, which could possibly lead to a slower stacking fault reduction during Cu-deposition , and thereby to a higher initial density of stacking faults in the samples with NaF prior to the annealing (see Supplemental Material S.7 for details). The last possibility can be considered in the simulation: an adjustment of the simulation to the experimental data of the samples without NaF is achieved by adapting the parameter set used for the simulation in Fig. 3(b) with lower initial expectation values for the stacking fault fraction of $p^{exp} = 1.63$ % (Fig. 3(h)) and $p^{exp} = 1.1\%$ (Fig. 3(i)) and an increase of the energy distribution parameter μ_E from

2.5 to $\mu_E = 5$. The change of μ_E improves the agreement with the experimental data at the later stage of the simulation, but cannot be used to draw conclusions on the real energy distribution due to the simplified nature of the model. In the last stage of the simulation the limited thickness of the thin film could become relevant. The difference between a simulation with two and three dimensional grain growth and the effect of a μ_E variation on the energy density distribution is illustrated in the Supplemental Material S.4.8 and S.4.9.

In summary, the results in Fig. 3 show that our grain growth model can reproduce the decrease of stacking faults in various CIS samples during annealing with different heating rates, supporting the hypothesis of the influence of a stacking fault driving force on grain growth as the decisive mechanism for stacking fault annihilation in CIGS growth by co-evaporation.

C. Estimation of annealing time for stacking fault annihilation at constant temperature

For manufacturing purposes it is interesting to predict at which temperatures and for how long a Cu-poor CIS thin film has to be annealed to annihilate stacking faults without passing through a Cu-rich process step. To approach this problem, we perform simulations at constant temperatures. We use parameter sets which produce simulations with good agreement to the experimental data of the samples A and C with and without NaF (Tab. A.I, modified with Q = 3.11 eV, p^{exp} = 10 % and p^{exp} = 1.1 %). Fig. 5 shows the evolution of the energy density E_{vw} at different annealing temperatures for a simulation time of five hours.

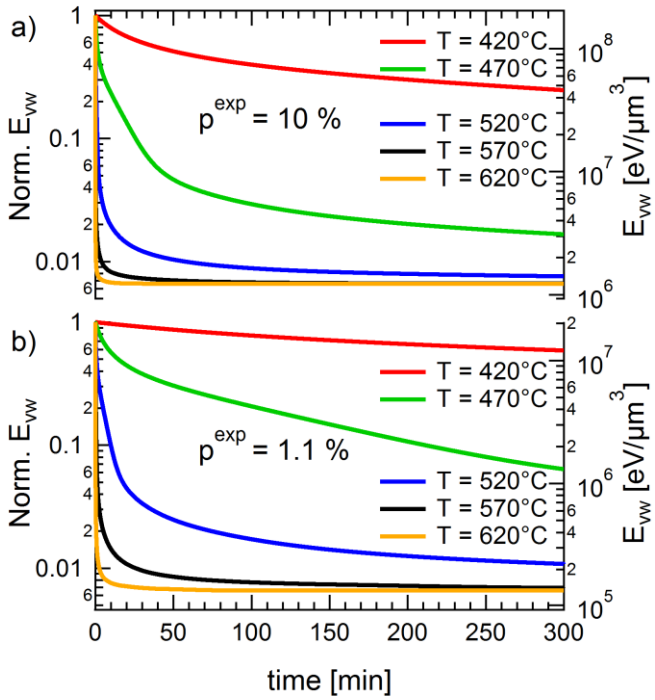

Fig. 5: Simulation of stacking fault energy density E_{vw} during annealing at various constant temperatures for five hours. (a) Initial expectation value of the stacking fault fraction p^{exp} = 10 %, (b) p^{exp} = 1.1 %

At higher annealing temperatures the energy density E_{vw} decreases more rapidly. The remaining E_{vw} fraction after five hours is smaller for higher annealing temperatures, but the effect of additional annealing time becomes negligible for temperatures > 520°C. While the relative decrease is faster for the higher initial expectation value of the stacking fault content p^{exp} = 10 %, the remaining absolute energy density after identical annealing times is still lower for the smaller initial energy density with p^{exp} = 1.1 %. The annealing times required in the simulation to reach 50 %, 10 % and 5 % of the initial energy density are given in Table II.

Tab. II: Annealing times for the reduction of the stacking fault energy density E_{vw} to a fraction of the initial value. Values for simulations with initial parameter set and activation energy Q = *3.11 eV, expectation values of the stacking fault fraction p^{exp} = 10 % and p^{exp} = 1.1 %.*

T [°C]	50 % Intensity	10 % Intensity	5 % Intensity	50 % Intensity	10 % Intensity	5 % Intensity
	Initial p^{exp} = 10 %			Initial p^{exp} = 1.1 %		
420	49 min 56 s	>5 h	>5 h	>5 h	>5 h	>5 h
470	1 min 42 s	27 min 4 s	48 min 15 s	15 min 48 s	2 h 35 min 6s	>5 h
520	5 s	1 min 24 s	2 min 31 s	50 s	11 min 12 s	20 min 12 s
570	0.4 s	6 s	11 s	4 s	50 s	1 min 30 s
620	0.04 s	0.6 s	1 s	0.4 s	5 s	8 s

At the considered stacking fault densities, annealing temperatures ≥ 570 °C appear necessary for the reduction of stacking faults to less than 1 % of the original value within several minutes, which is a realistic time frame for production purposes. Further temperature increases only lead to marginal improvements. The remainder of a small fraction of stacking faults is in accordance with previous results on the evolution of the stacking fault feature during Cu-Se deposition at various temperatures, where even for 530°C a small stacking fault fraction remained, which only disappeared at the Cu-poor-Cu-rich transition [13]. Previous experimental data from CIS thin films without NaF annealed at a constant temperature of 420°C [29] show a decrease of the stacking fault feature to 68 % - 80 % of the original value after 30 min annealing, while the simulation predicts a decrease to 91 % ($p^{exp} = 1.1$ %). The 10 % - 20 % underestimation of the decrease of the stacking fault feature by the simulation could be attributed to the presence of additional grain growth mechanisms not included in the model, such as stress relaxation [27], surface energy [39], energetically favored grain shapes and diffusion-induced grain boundary migration [29]. When applying the simulation results to real processes in different deposition chambers, one would have to keep in mind the possibility of a systematic uncertainty of the temperature measurement of the experiments we use to adapt the model parameters. Also, a sufficient Se background pressure has to be provided to avoid Se loss during annealing [46].

IV. CONCLUSION

We show by *in-situ* synchrotron X-ray diffraction of Cu-poor $CuInSe_2$ thin films that a strong reduction of stacking faults can be achieved by annealing without passing through a Cu-rich film composition during deposition via co-evaporation. By adapting a simple numerical model to describe grain growth driven by stacking fault energy and grain boundary curvature in polycrystalline $CuInSe_2$ thin films during annealing, a good agreement with the experimental *in-situ* XRD data is achieved, supporting the hypothesis of stacking fault reduction through grain growth. When using substrates, such as polyimide foils, which require temperatures below 450°C, annealing is not an alternative to a Cu-rich intermediate process step for the reduction of stacking faults. However, the simulations predict that high temperatures above 570°C allow a substantial reduction of stacking faults via annealing.

SUPPLEMENTAL MATERIAL

Supplemental material with details on the phase field simulation, exemplary STEM images, more information on the grain growth model (derivation of the critical radius r*, the critical energy E*, overview of the model parameters and estimation of their initial value, comparison of two- and three-dimensional simulations, reproducibility and volume change) and the effect of a variation of the parameters on the simulation, as well as a more detailed discussion of the possible effect of Na, is available online:

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APPENDIX

The value of the geometrical factor φ is estimated to be 1 for three-dimensional grains [37]. And for the spherical grain shape assumed in our simple model the shape factor is $\phi = 1$. The starting values for the free energy of the grain boundary $\gamma = 0.1\ \mathrm{J/m^2}$, the activation energy $Q = 3.3$ eV, the grain size distribution parameters $\mu_d = 2.5$, $\sigma_d = 0.5$ and the initial expected grain size $d^{exp} = 250$ nm are based on experimental and theoretical data [47, 48, 36, 41, 14]. We assume that for small fractions (≤ 10 %) of faulted planes, the energy density of a grain is proportional to the percentage p of faulted 112 planes in a grain – not taking into account the effects of adjacent and accumulated stacking faults on the energy. This means the expectation value of the energy density E^{exp} is calculated by multiplying the expectation value of the stacking fault fraction p^{exp} with a proportionality factor $E_{100\%}$, which corresponds to the extrapolated case that all lattice planes are faulted: $E^{exp} = E_{100\%} \cdot p^{exp}$. The proportionality factor $E_{100\%}$ is calculated by multiplying the area energy density of a faulted plane with the reciprocal value of the 112 lattice plane distance $d_{112} = 3.3453$ Å (ICDD card 01-81-1936) of CIS. Theoretical values for

the energy of intrinsic stacking faults in CIS range from $0.09\ \mathrm{J/m^2}$ to $0.11\ \mathrm{J/m^2}$ [1]. We use a stacking fault energy of $E_{SF} = 0.10\ \mathrm{J/m^2}$, resulting in a value for the proportionality factor of $E_{100\%} = 1.87 \cdot 10^9 \mathrm{eV/\mu m^3}$. As initial value, we assume an expectation value of $p^{exp} = 10\ \%$ for the stacking fault fraction. The stacking fault densities in our model might be slightly overestimated because the model does not include the energy associated with the existence of dislocations at the end of stacking faults which do not terminate in grain boundaries (see Supplemental Materials S.4.7 for an estimation of the contribution of the dislocation energy). With $\mu_E = \mu_a = 2.5$ and $\sigma_E = \sigma_a = 0.5$ we produce initial grain size and energy density distributions for an ensemble of 1 000 000 grains. The distributions are depicted in Fig. S2(a) and S2(b) in the Supplemental Material S.4. The temperature T in Eq. (5) is given by the temperature profiles applied during the annealing experiments. There are no literature values available for the grain boundary mobilities in CIS. Therefore, we use existing data for the mobility of aluminum grain boundaries at 800 K [49] and activation energy [50] to make a very rough estimation of the prefactor of the grain boundary mobility $M_0 = 2.55 \cdot 10^{10} \mathrm{\mu m^4/eV \cdot s}$ by resolving Eq. (5). This estimation has to be treated with caution, since the range of activation energy values in [50] is compatible with M_0 values varying by more than two orders of magnitude. Also, the mobility M and the activation energy Q are given in both references for a range of <111> tilt grain boundaries with specific misorientation angles, and we are interested in an average value for all grain boundaries. The resulting initial parameter set is summarized in Table A.I.

Tab. A.I: Initial parameter set for the grain growth simulation.

Parameter	*Initial value*
Shape factor of k_r: φ	1
Geometrical factor of k_E: ϕ	1
Free energy of the grain boundary: γ	$0.1 \frac{\mathrm{J}}{\mathrm{m^2}}$
Activation energy: Q	3.3 eV
Prefactor of the grain boundary mobility: M_0	$2.55 \cdot 10^{10} \frac{\mu\mathrm{m}^4}{\mathrm{eV \cdot s}}$
Experimentally measured sample temperature: T	Experimental
Initial expectation value of the grain diameter: d^{exp}	250 nm
Grain size distribution parameter: μ_d	2.5
Grain size distribution parameter: σ_d	0.5
Proportionality factor for the conversion of a stacking fault ratio to an energy value: $E_{100\%}$	$1.87 \cdot 10^9 \frac{\mathrm{eV}}{\mu\mathrm{m}^3}$
Initial expectation value for the stacking fault ratio: p^{exp}	10 %
Energy distribution parameter: μ_E	2.5

Energy distribution parameter: σ_E	0.5

REFERENCES

[1] N. I. Medvedeva, E. V. Shalaeva, M. V. Kuznetsov, and M.V. Yakushev, Phys. Rev. B 73, 035207 (2006).

[2] A. W. Vere, S. Cole, and D. J. Williams, Journal of Electron. Mater. 12, 551 (1983).

[3] Y. Yan, G. M. Dalpian, M. M. Al-Jassim, and S.-H. Wei, Phys. Rev. B 70, 193206 (2004).

[4] L. C. Qin, D. X. Li, and K. H. Kuo, Philos. Mag. A 53, 543 (1986).

[5] J. Pohl, M.Müller, A. Seidl, and K. Albe, J. Cryst. Growth 312, 1411 (2010).

[6] Y. Yan, K. Jones, C. Jiang, X. Wu, R. Noufi, and M. Al-Jassim, Physica B 25, 401 (2007).

[7] Y. Yan, M. M. Al-Jassim, K. M. Jones, S.-H. Wei, and S. B. Zhang, Appl. Phys. Lett. 77 1461 (2000).

[8] H. Mirhosseini, J. Kiss and C. Felser, Phy. Rev. Appl. 4, 064005 (2015).

[9] E. Simsek Sanli, Q. M. Ramasse, W. Sigle, D. Abou-Ras, R. Mainz, A. Weber, H.-J. Kleebe, and P. A. van Aken, J. Appl. Phys.120, 20531 (2016).

[10] E. Simsek Sanli, D. Barragan-Yani, Q. M. Ramasse, K. Albe, R. Mainz, D. Abou-Ras, A. Weber, H.-J. Kleebe, and P. A. van Aken, Phys. Rev. B. 95, 195209 (2017).

[11] C. Lei, C-M. Li, A. Rockett, I.M. Robertson, and W. Shafarman, Mater. Res. Soc. Symp. Proc. Vol. 865, F4.3.1 (2005)

[12] T. Wada, T. Negami, and M. Nishitani, J. Mater. Res. 9, 658 (1994)

[13] R. Mainz, E. Simsek Sanli, H. Stange, D. Azulay, S. Brunken, D. Greiner, S. Hajaj, M. D. Heinemann, C. A. Kaufmann, M. Klaus, Q. M. Ramasse, H. Rodriguez-Alvarez, A. Weber, I. Balberg, O. Millo, P. A. van Aken and D. Abou-Ras, Energy Environ. Sci. 9, 1818 (2016).

[14] H. Stange, S.Brunken, H.Hempel, H. Rodriguez-Alvarez, N. Schäfer, D. Greiner, A.Scheu, J. Lauche, C. A. Kaufmann, T. Unold, D. Abou-Ras, and R. Mainz, Appl. Phys. Lett. 107, 152103 (2015).

[15] H. Rodriguez-Alvarez, N. Barreau, C. Kaufmann, A. Weber, M. Klaus, T. Painchaud, H.-W. Schock, and R. Mainz, Acta Mat. 61, 4347 (2013).

[16] T. Kato, J.-L. Wu, Y. Hirai, H. Sugimoto, and V. Bermudez, IEEE Journal of Photovoltaics, (2018)

[17] A. M. Gabor, J. R. Tuttle, D. S. Albin, M. A. Contreras, and R. Noufi, Appl. Phys. Lett. 65, 198 (1994).

[18] R. Caballero, C. A. Kaufmann, V. Efimova, T. Rissom, V. Hoffmann, and H. W. Schock, Prog.Photovolt. 21, 30 (2013).

[19] A. Chirila, S. Buecheler, F. Pianezzi, P. Bloesch, C. Gretener, A. R. Uhl, C. Fella, L. Kranz, J. Perrenoud, S. Seyrling, R. Verma, S. Nishiwaki, Y. E. Romanyuk, G. Bilger, and A. N. Tiwari, Nature Materials 10, 857 (2011)

[20] T. Feurer, P. Reinhard, E. Avancini, B. Bissig, J. Löckinger, P. Fuchs, R. Carron, T. P. Weiss, J. Perrenoud, S. Stutterheim, S. Buecheler, and A. N. Tiwari, Prog. Photovolt: Res. Appl. 25, 645 (2017)

[21] R. Caballero, C. A. Kaufmann, T. Eisenbarth, T. Unold, R. Klenk, and H.-W. Schock, Prog. Photovolt. 29, 547 (2011)

[22] A. Chirila, P. Reinhard, F. Pianezzi, P. Bloesch, A. R. Uhl, C. Fella, L. Kranz, D. Keller, C. Gretener, H. Hagendorfer, D. Jaeger, R. Erni, S. Nishiwaki, S. Buecheler, and A. N. Tiwari, Nature Materials 12, 1107 (2013)

[23] W.-S. Seo, C.-H. Pai, K. Koumoto, and H. Yanagida, J. Ceramic Soc. J. 99, 443 (1991).

[24] A. M. Deus, M. A. Fortes, P. J. Ferreira, and J. B. Vander Sande, Acta Mat. 50, 3317 (2002).

[25] C. Genzel, I. Denks, J. Gibmeier, M. Klaus, and G. Wagener, Nucl. Instrum. Methods A 578, 23 (2007).

[26] C. Genzel, I. A. Denks, R. Coelho, D. Thomas, R. Mainz, D. Apel, and M. Klaus, J. Strain Anal. Eng. Des. 46, 615 (2011).

[27] R. Mainz, H. Rodriguez-Alvarez, M. Klaus, D. Thomas, J. Lauche, A. Weber, M. D. Heinemann, S. Brunken, D. Greiner, C. A. Kaufmann, T. Unold, H.-W. Schock, and C. Genzel, Phys. Rev. B 92, 155310 (2015).

[28] H. Rodriguez-Alvarez, A.Weber, J. Lauche, C. A. Kaufmann, T. Rissom, D. Greiner, M. Klaus, T. Unold, C. Genzel, H.-W. Schock, and R. Mainz, Adv. Energy Mater. 3, 1381 (2013).

[29] H. Stange, S. Brunken, D. Greiner, M. D. Heinemann, C. A. Kaufmann, S. S. Schmidt, J-.P. Bäcker, M. Klaus, C. Genzel, and R. Mainz, Acta Mat. 111, 377 (2016).

[30] G. Kaune, S. Hartnauer, and R. Scheer, Physica Status Solidi A 211, 1991 (2014).

[31] P. Pistor, S. Zahedi-Azad, S. Hartnauer, L. A. Wägele, E. Jarzembowski, and R. Scheer, Physica Status Solidi A 212, 1897 (2015).

[32] D. Güttler, A. Chirila, S. Seyrling, P. Blosch, S. Buecheler, X. Fontane, V. Izquierdo-Roca, L. Calvo-Barrio, A. Perez-Rodriguez, J. Morante, A. Eicke, and A. Tiwari, in Proceedings of the 35th IEEE Photovoltaic Specialists Conference, Honolulu, p. 3420, (2010).

[33] A. M. Gabor, J. R. Tuttle, A. Schwartzlander, A. L. Tennant, M. A. Contreras and R. Noufi, in Proceedings of the 24th IEEE Photovoltaic Specialists Conference, Waikoloa, p.83, (1994).

[34] S. Nishiwaki, T. Satoh, S. Hayashi, Y. Hashimoto, T. Negami and T. Wada, J. Mat. Res. 14, 4514 (1999)

[35] C. V. Thompson, Annu. Rev. Mater. Sci. 20, 245 (1990).

[36] T. Schlenker, M. Luis-Valero, and H.W. Schock, J. H. Werner, J. Cryst. Growth 264, 178 (2004).

[37] M. Hillert, Acta Metall. 13, 227 (1965).

[38] G. Gottstein, *Materialwissenschaft und Werkstofftechnik*, Springer-Vieweg, Wiesbaden, (2014).

[39] C. V. Thompson, Interface Sci. 6, 85 (1998).

[40] C. Li, E. Simsek Sanli, H. Stange, M. D. Heinemann, D. Greiner, N. Schäfer, R. Mainz, W. Sigle, D. Abou-Ras and P. A. van Aken, Proceedings of the 2018 Microscopy & Microanalysis Conference, Microsc. Microanal. 24 (Suppl 1), 1492, doi 10.1017/S1431927618007948 (2018)

[41] D. Abou-Ras, S. Schorr, and H. W. Schock, J. Appl. Cryst. 40, 841 (2007).

[42] E. Cadel, N.Barreau, J. Kessler, and P. Pareige, Acta Mat. 58, 2634 (2010).

[43] O. Cojocaru-Mirédin, P. Choi, R. Wuerz, and D. Raabe, Ultramicroscopy 11, 552 (2011).

[44] G. Gottstein and L.S. Shvindlerman, *Grain Boundary Migration in Metals*, CRC Press, Boca Raton, (2014)

[45] D. Colombara, F. Werner, T. Schwarz, I. Cañero Infante, Y. Fleming, N. Valle, C. Spindler, E. Vacchieri, G. Rey, M. Guennou, M. Bouttemy, A. Garzón Manjón, I. Peral Alonso, M. Melchiorre, B. El Adib, B. Gault, D. Raabe, P. J. Dale and S. Siebentritt, Nature Communications 9, 826 (2018)

[46] J. J. Scragg, P. J. Dale, D. Colombara and L. M. Peters, ChemPhysChem Vol. 13, 3035 (2012)

[47] A. Praveen Kumar, and K. V. Reddy, Thin Solid Films 304, 365 (1997).

[48] H. Yamaguchi, H. Hiramatsu, H. Hosono, and T. Mizoguchi, Appl. Phys. Lett. 104, 153904 (2014).

[49] K. G. F. Janssens, D. Olmsted, E. A. Holm, S. M. Foiles, S. J. Plimpton, and P. M. Derlet, Nature Materials 5, 124 (2006).

[50] G. Gottstein, D. Molodov, U. Czubayko, and L. Shvindlerman, J. Phys. IV 05 (C3) C3-89-C3-106 (1995).